83323550

CONTROL DATA CORPORATION

CDC® FIXED MODULE DRIVE

BZ7E1

BZ7E2

GENERAL DESCRIPTION

OPERATION

THEORY OF OPERATION

HARDWARE REFERENCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A (5-29-80)	Manual Released. This edition obsoletes all previous editions.
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C (12-20-80)	Incorporate ECO PE61463 and ECO PE61340. Miscellaneous editorial and technical corrections. This edition obsoletes all previous editions.
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or use Comment Sheet in the back of this manual.

LIST OF EFFECTIVE PAGES

Sheet 1 of 2

New features, as well as changes, deletions, and additions to information in this manual are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV	PAGE	REV
Cover	-	Blank	-
Blank	-	S-2 Div	-
Title P	-	Blank	-
ii	E	2-1	A
iii	E	2-2	D
iv	E	2-3	D
v	A	2-4	C
vi	B	2-5	C
vii	A	2-6	C
viii	C	2-7	C
ix	C	2-8	C
x	E	2-9	C
xi	E	2-10	B
xii	B	2-11	C
S-1 Div	-	2-12	C
Blank	-	Blank	-
1-1	A	S-3 Div	-
1-2	A	Blank	-
1-3	B	3-1	B
1-4	A	3-2	B
1-5	A	3-3	C
1-6	C	3-4	C
1-7	A	3-5	C
1-8	A	3-6	C
1-9	B	3-7	C
1-10	B	3-8	A
1-11	C	3-9	C
1-12	A	3-10	C
1-13	C	3-11	C
1-14	C	3-12	A
1-15	B	3-13	B
1-16	C	3-14	C
1-17	B	3-15	C

LIST OF EFFECTIVE PAGES (Contd)

Sheet 2 of 2

PAGE	REV	PAGE	REV
3-16	C	3-51	E
3-17	C	3-52	C
3-18	C	3-53	C
3-19	A	3-54	E
3-20	C	3-55	E
3-21	C	3-56	E
3-22	C	3-57	E
3-23	C	3-58	E
3-24	C	3-59	E
3-25	C	3-60	E
3-26	C	3-61	E
3-27	C	3-62	E
3-28	C	3-63	E
3-29	C	3-64	E
3-30	C	3-65	E
3-31	C	3-66	E
3-32	C	3-67	E
3-33	C	3-68	E
3-34	C	3-69	E
3-35	C	3-70	E
3-36	C	3-71	E
3-37	C	3-72	E
3-38	C	3-73	E
3-39	C	3-74	E
3-40	C	3-75	E
3-41	C	3-76	E
3-42	C	3-77	E
3-43	C	3-78	E
3-44	C	3-79	E
3-45	C	Blank	-
3-46	C	Cmt Sht	-
3-47	C	Rtn Env	-
3-48	C	Blank	-
3-49	C	Cover	-
3-50	C		

PREFACE

INTRODUCTION

This manual contains reference information for technical personnel who will be installing and maintaining the BZ7E1/BZ7E2 Fixed Module Drive (FMD).

The configuration chart on the next page lists the various models available for each of the FMDs, together with the specific feature groupings that distinguish one from the other.

MANUAL ORGANIZATION

Information in this manual is divided into three sections:

Section 1 - General Description: Describes equipment functions, specifications, and physical description.

Section 2 - Operation: Describes and illustrates the location and use of all controls and indicators; also provides operating instructions.

Section 3 - Theory of Operation: Describes basic logic and mechanical functions.

OTHER MANUALS

Additional information on the FMD is given in the following manuals:

PUBLICATION NO.	TITLE
83323560	Hardware Maintenance Volume 1: installation and checkout, preventive and corrective maintenance, and parts data.
83323570	Hardware Maintenance Volume 2: logic diagrams, assembly diagrams, and backpanel wire lists for the FMD.

83323580	Troubleshooting: Device micro-diagnostic test descriptions, operating procedures, error code dictionary, and corrective action.
83322440	CDC Microcircuits Manual

CONFIGURATION CHART

MODEL	FREQUENCY		FIXED HEADS INSTALLED	ROUND/FLAT I/O CABLE	SINGLE/DUAL CHANNEL
	60 Hz	50 Hz			
BZ7E1-A	X		No	Round	Single
-B		X	No	Round	Single
-C	X		No	Flat	Single
-D		X	No	Flat	Single
-E	X		Yes	Round	Single
-F		X	Yes	Round	Single
-G	X		Yes	Flat	Single
-H		X	Yes	Flat	Single
-J	X		No	Flat	Single
-K		X	No	Flat	Single
BZ7E2-A	X		No	Round	Dual
-B		X	No	Round	Dual
-C	X		No	Flat	Dual
-D		X	No	Flat	Dual
-E	X		Yes	Round	Dual
-F		X	Yes	Round	Dual
-G	X		Yes	Flat	Dual
-H		X	Yes	Flat	Dual

CONTENTS

FIGURES

TABLES

ABBREVIATIONS

ABR	Absolute Reserve	MH	Movable Head
AM	Address Mark	MPU	Microprocessing Unit
AMP	Amplifier	NRM	Normal
AMPL	Amplifier	NRZ	Non-Return to Zero
BKR	Breaker	PIA	Peripheral Interface Adapter
CNTR	Counter	PLO	Phase-Locked Oscillator
CONTR	Controller	PWR	Power
DAC	Digital-to-Analog Converter	RAM	Random Access Memory
		RCVR	Receiver
DIFF	Differential	RD	Read
DI/DII	Disable (Chan I/II)	REG	Register
FH	Fixed Head	ROM	Read-Only Memory
GEN	Generator	RTM	Reserve Timeout
HD	Head	RTZ	Return to Zero
HDA	Head & Disk Assembly	SEL	Select
I/O	Input/Output	VMA	Valid Memory Address
LED	Light Emitting Diode	WRT	Write
MFM	Modified Frequency Modulation	XMTR	Transmitter
		XTAL	Crystal

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

The BZ7E1/BZ7E2 Fixed Module Drive (FMD) is a high speed random access storage facility that provides up to 675 megabytes of direct access storage. The unit (see figure 1-1) consists of a standalone cabinet and frame containing a head/disk assembly (HDA), drive motor and brake, power supplies, and a logic chassis.

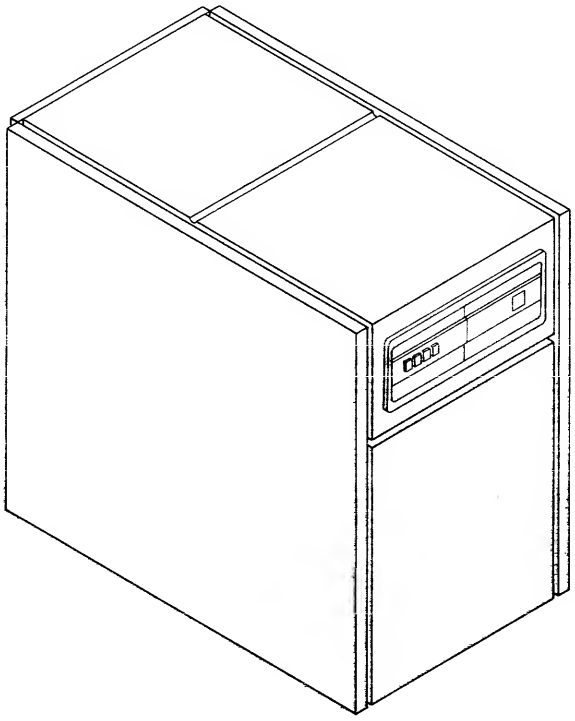


Figure 1-1. Fixed Module Drive (FMD)

STANDARD OPTIONS

The standard options available on the FMD will vary from one model to another. The configuration chart (located in the front of this manual) lists the optional features included with each model.

FIXED HEAD FEATURE

The fixed head feature adds 96 fixed heads to the FMD. The fixed heads provide an additional 1.9 megabytes of zero seek time storage capacity to the FMD.

DUAL CHANNEL FEATURE

The dual channel feature permits two controllers to have access to the same device. Either controller can select and reserve the device. Once selected and/or reserved, the device becomes busy to the opposite controller. The device is released by issuing a Release command on the active interface or automatically after 500 milliseconds of channel inactivity, provided the Release Timer Select switch at location A07 on the logic chassis is set to RTM. A Priority Select on the inactive channel can force a selection by disabling the channel to the controller having the drive selected or reserved.

SPECIFICATIONS

The physical, environmental, power requirements, and performance characteristics are listed in table 1-1.

EQUIPMENT PHYSICAL DESCRIPTION

GENERAL

Figure 1-2 identifies the physical location of the major assemblies and components that comprise the unit. Many, but not all, of these assemblies and components have been assigned physical location codes. The primary location codes are as follows:

- A1 - AC Power Supply
- A2 - DC Power Supply
- A3 - Logic Chassis
- A4 - Drive Motor
- A5 - Operator Panel
- A6 - Diagnostic Control Panel
- A7 - Deck
- A8 - I/O Panel (round cable configuration)
- A8 - I/O Bracket (flat cable configuration)
- A9 - Frame and Frame Components
- A10 - Blower

TABLE 1-1. FIXED MODULE DRIVE SPECIFICATIONS

Characteristics	Conditions	Specifications
	PHYSICAL	
Size	Height	920 mm (36 in)
	Width	584 mm (23 in)
	Depth	965 mm (38 in)
	Weight	290 kg (639 lb)
HDA	Number of disks	12
	Movable data heads	40
	Servo Heads	1
	Tracks per inch	662
	Fixed data heads	96
	Physical heads per surface	2
	Movable head logical cylinders	843 (0-842)
	ENVIRONMENTAL	
Temperature		
Storage	Range	-10°C to 50°C (14°F to 122°F)

Table Continued on Next Page

TABLE 1-1. FIXED MODULE DRIVE SPECIFICATIONS (Contd)

Characteristics	Conditions	Specifications
	Maximum change	15°C (27°F) per hour
Transit	Range	-40°C to 70°C (-40°F to 158°F)
	Maximum change	20°C (36°F) per hour
Non-operating	Range	10°C to 35°C (50°F to 95°F)
	Maximum change	10°C (18°F) per hour
	Gradient	10°C (18°F)
Operating	Range	10°C to 35°C (50°F to 95°F)
	Maximum change	10°C (18°F) per hour
	Gradient	10°C (18°F)
Humidity	Storage	10% to 90%, no condensation
	Transit	0% to 100% RH, no condensation
	Non-operating	20% to 80% RH, no condensation 10% per hour maximum change
	Operating	20% to 80% RH, no condensation 10% per hour maximum change

Table Continued on Next Page

TABLE 1-1. FIXED MODULE DRIVE SPECIFICATIONS (Contd)

Characteristics	Conditions	Specifications
Barometric Pressure Standard Day	Storage/ Non-Operating	-300 m to 2500 m (-980 ft to 8200 ft) 104.69 kPa to 73.96 kPa (31 in to 21.9 in Hg)
	Transit	-300 m to 2500 m (-980 ft to 8200 ft) 104.69 kPa to 73.96 kPa (31 in Hg to 21.9 in Hg)
	Operating	-300 m to 2000 m (-980 ft to 6560 ft) 104.69 kPa to 79.36 kPa (31 in Hg to 23.5 in Hg)
Air Cleanliness	Storage/Transit Non-operating/	Same as operating with proper packing
	Non-operating/ operating	Particle size (microns) — Particles m^3 More than 1: $4x10^7$ More than 1.5: $4x10^6$ More than 5: $4x10^5$ Sulpher dioxide: 0.14 parts per million maximum

Table Continued on Next Page

TABLE 1-1. FIXED MODULE DRIVE SPECIFICATIONS (Contd)

Characteristics	Conditions	Specifications
POWER REQUIREMENTS		
AC Power Input	60 (+0.6, -1)Hz	208 (+15, -29) V (Ø-Ø) 230 (+16, -32) V (Ø-Ø)
	50 (+0.5,-1) Hz	220 (+15,-22) V (Ø-N)
		240 (+17,-24) V (Ø-N)
Power	Carriage and Disks in Motion	208 V: 1400 W (4760 Btu/h) with maximum line current of 6.7 A.
		220 V: 1300 W (4420 Btu/h) with maximum line current of 5.9 A.
	Carriage and Disks at Rest	208 V: 650 W (2210 Btu/h) with maximum line current of 3.1 A.
		220 V: 600 W (2040 Btu/h) with maximum line current of 2.7 A.
PERFORMANCE		
Transfer rate	Disk speed	9.677 MHz (1 209 625 bytes/s)
Latency	at 3600 r/min	Latency is time to reach a particular track address after positioning is complete.

Table Continued on Next Page

TABLE 1-1. FIXED MODULE DRIVE SPECIFICATIONS (Contd)

Characteristics	Conditions	Specifications
	Average	8.33 milliseconds (disk rotation speed at 3600 r/min)
	Maximum	17.3 milliseconds (disk rotation speed at 3474 r/min)
Recording	Mode	Modified frequency modulation (MFM).
	Density-inner track	2534 bits/cm (6417 bits per inch)
Seek Time	Full	50 milliseconds maximum
	Average	25 milliseconds
	Single Track	10 milliseconds maximum

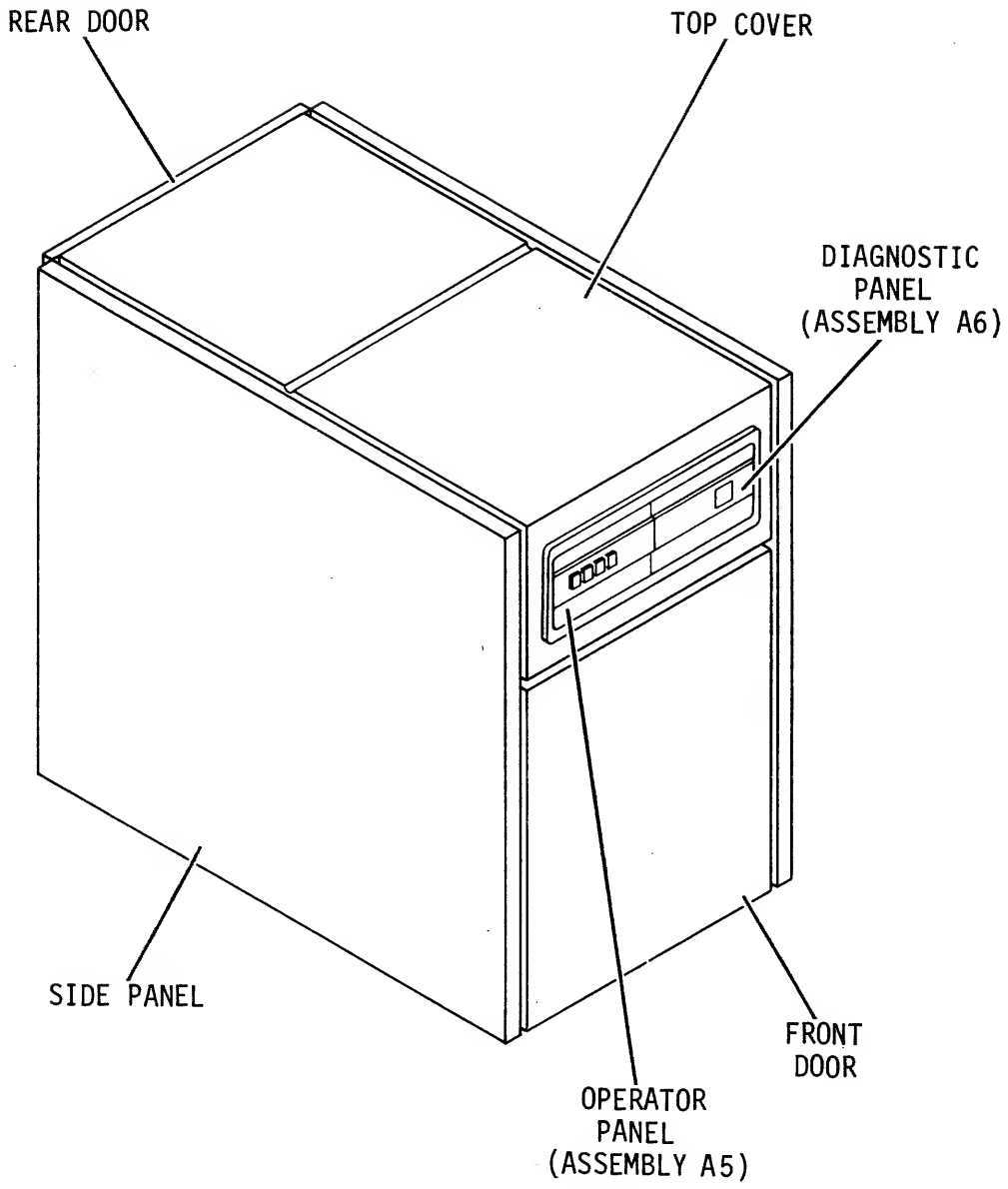


Figure 1-2. Major Assemblies (Sheet 1 of 3)

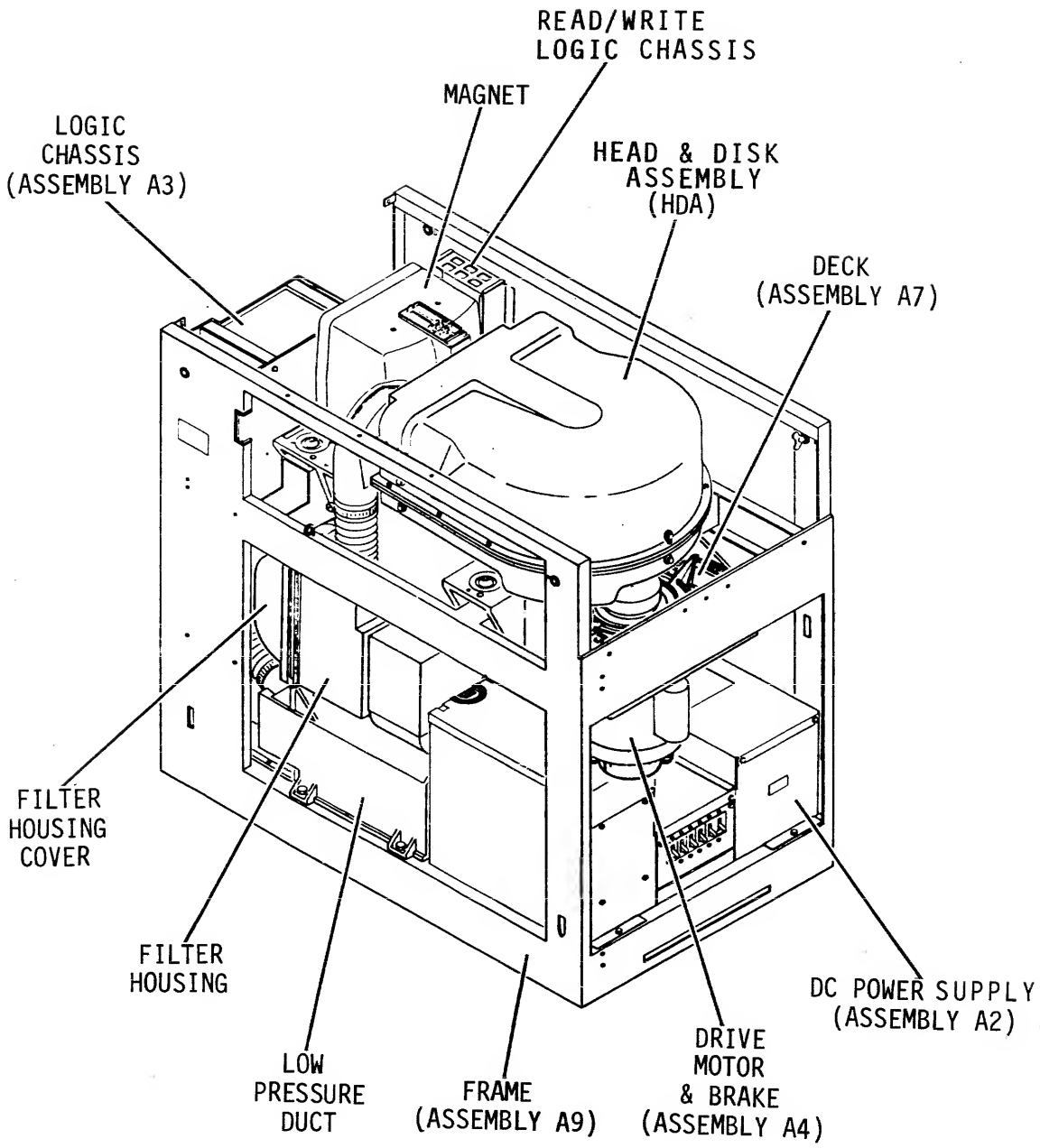
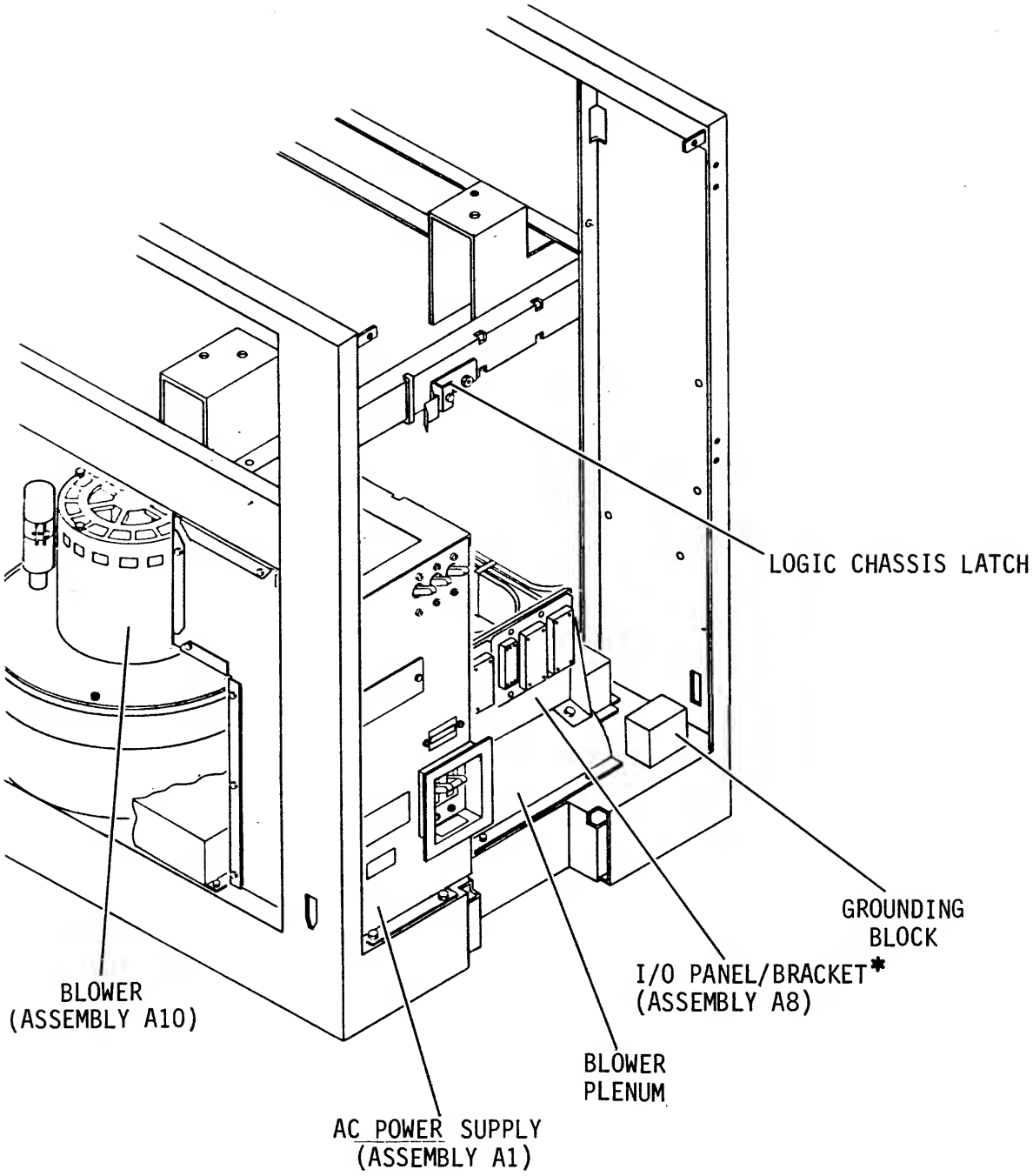


Figure 1-2. Major Assemblies (Sheet 2)



* ILLUSTRATION SHOWS I/O PANEL USED FOR ROUND CABLE INTERFACE. I/O BRACKET IS SUBSTITUTED FOR I/O PANEL TO ACCOMODATE FLAT CABLE INTERFACE.

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Figure 1-2. Major Assemblies (Sheet 3)

HEAD AND DISK ASSEMBLY (HDA)

The HDA (figure 1-3) is an enclosed disk pack that can be removed only by field service personnel. It contains 40 read/write heads (used to read and write system data) and one servo head. All of the movable heads are attached to a positioning mechanism, referred to as a carriage, that is moved by a voice coil motor.

An HDA configured with the fixed head feature has an additional 96 fixed read/write heads. These heads are mounted opposite the lower surface of the bottom disk (disk 0).

The HDA contains a spindle that rotates 12 magnetic coated disks. The spindle has an exposed pulley at the bottom of the HDA. The pulley, in turn, is driven by a motor that is part of the deck. Normal disk rotation is 3600 revolutions per minute. Direction of rotation is counterclockwise as viewed from the top of the HDA.

When the HDA is not in use, the heads rest on the disk surface in preassigned landing zones located on the outer area of the disk surface. As the disks rotate and come up to speed, the heads fly on a cushion of air close to the disk surface.

The servo surface contains prerecorded servo position tracks used to define the physical location of the movable read/write heads, and to derive machine clock, index, and rotational position sensing (sector) timing signals. The servo surface is monitored by one read-only head. Servo data is prerecorded at the factory and cannot be modified in the field.

A1 - AC POWER SUPPLY

The ac power supply provides power to the dc power supply, the blower motor, and the drive motor. In addition, the ac power supply generates the +5 V MPU and +24Y dc power required to operate the diagnostic and operator panel switch/indicators, the basic logic power used by the MPU test and diagnostic memory card in the logic chassis, and the power control relays.

The +5 V MPU power supply is adjustable via a potentiometer located on _VLV card in the ac power supply.

The MAIN subsystem contactor (CB1) is located within the ac power supply. If the MAIN contactor opens, all ac power and dc power is removed from the unit.

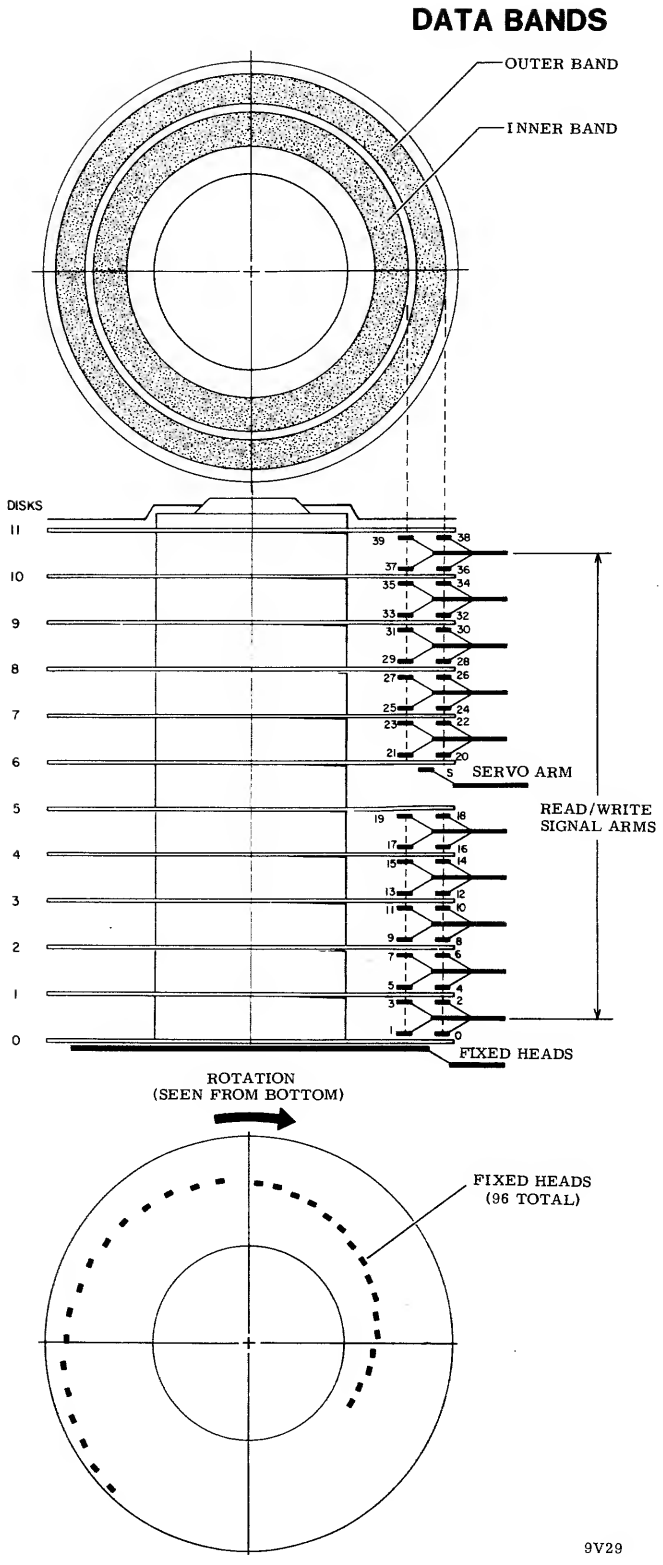

Figure 1-3. Head and Disk Assembly

A2 - DC POWER SUPPLY

The dc power supply provides the following dc voltages:

- ±10 V (regulated to ±5 V) to the logic chassis, HDA, and voltage sensing circuits
- ±24 V to the servo and read/write circuits
- +24X V to operate the ±5 V regulator board
- -36 V to the servo power amplifier within the dc power supply.

All of the dc voltages are protected by circuit breakers. In addition, the +5 and -5 V power supplies are adjustable via potentiometers located on the _GDV board inside the dc power supply.

A thermal breaker mounted on the _GDV board detects an over-temperature condition. If a temperature exceeding 135°C (275°F) is detected, it opens to break the interlock. The microprocessor on the test and diagnostic card drops all power to the unit (except for the blower and diagnostic logic) in the event of an over-temperature condition, or the loss of ±10, ±24 or -36 V power. If an over-temperature condition, or the loss of ±10 V, ±24 V, or -36 V is sensed by the microprocessor (MPU) on the test and diagnostic card (B03/C03), the MPU drops all power on the affected unit except for the blower and the diagnostic logic. Each of the above error conditions causes a unique error code to be generated by the test and diagnostic microprocesser and displayed on the diagnostic panel.

The dc power supply also contains a power amplifier board used to provide control current to the voice coil motor.

A3 - LOGIC CHASSIS

The logic chassis mounts and interconnects the logic cards. It is hinge mounted and swings out for easy access to the cards.

The logic chassis has three rows: A, B, and C. Rows A and C contain 9 slots; Row B contains 8 slots. Only eight slots are used for logic cards. Slot 9 is used for interconnections to the logic chassis.

Other quick-connect type connectors located along the side of the backpanel near row 9 are used to supply ±24 V, ±5 V, and ground.

A4 - DRIVE MOTOR

A capacitive start single-phase motor is used to rotate the spindle in the HDA. The motor is equipped with a fail-safe brake and is protected by a manually-resettable thermal breaker. Opening the drive motor thermal breaker causes a unique error code to be generated by the test and diagnostic microprocesser, and displayed on the diagnostic panel.

A5 - OPERATOR PANEL

The operator panel contains all of the switches and indicators needed by the operator. The switches and indicators are described in section 2 of this manual.

A6 - DIAGNOSTIC CONTROL PANEL

Automatically displays errors and status occuring during power up/down sequencing, as the result of power supply failure, or as the result of servo or logic malfunction. Errors and status are displayed as a four-digit hexadecimal code.

A7 - DECK

The deck provides a mounting surface for the drive motor, magnet assembly, HDA, and read/write electronics. The read/write chassis contains two cards that perform some of the read/write functions; the remaining read/write functions are performed by the cards in the main logic chassis.

An air pressure switch mounted in the air plenum senses the air flow entering the HDA. Failure to detect air flow cause the test and diagnostic microprocesser to drop power to the spindle motor and dc power supply. The condition also causes a unique error code to be displayed on the diagnostic panel.

A8 - I/O PANEL/BRACKET

The I/O panel provides a centralized place for the installation of external round I/O cables. Units configured for flat cable interface are equipped with a bracket in place of the I/O panel. External flat I/O cables are attached directly to the card at location A08 (channel 1), or location B08 (channel 2).

Each channel connection requires an "A" cable containing control lines, and a "B" cable containing data and servo clock information.

A9 - FRAME AND FRAME COMPONENTS

The frame supports and contains all unit assemblies.

A10 - BLOWER

The blower provides cooling air to the power supplies, the logic chassis, and the HDA. Refer to the pressure switch description under A7 deck assembly.

EQUIPMENT FUNCTIONAL DESCRIPTION

GENERAL

Figure 1-4 is a block diagram of the drive. When operating in remote mode (Local/Remote switch on card in slot B03/C03 set to up position), the controller must enable the power sequence circuit. The power sequence circuit enables power to the spindle motors and power supplies on all of the drives connected to the controller.

Unit selection commands are placed on the Unit Select bus accompanied by the Unit Select Tag. The Unit Select bus lines are binary-coded to select 1 of 16 devices.

Commands other than unit selection placed on bus out Bits 0-9 and Tag lines 2^0-2^3 move the read/write heads to the selected location on the disk surface and initiate transmission of data to or from the disk surface. The controller may request status responses from the drive before and after each operation. Data is stored or retrieved from a particular head and rotational position on the disk.

INTERFACE DESCRIPTION

The drive can communicate only with the controller. The interface is provided by two cables for a single channel unit and by four cables for a dual channel unit. The controller issues all commands to the drive. Tag signals define the basic type of operation to be performed. Device bus out signals (Bits 0 through 9) further modify or define basic commands selected by

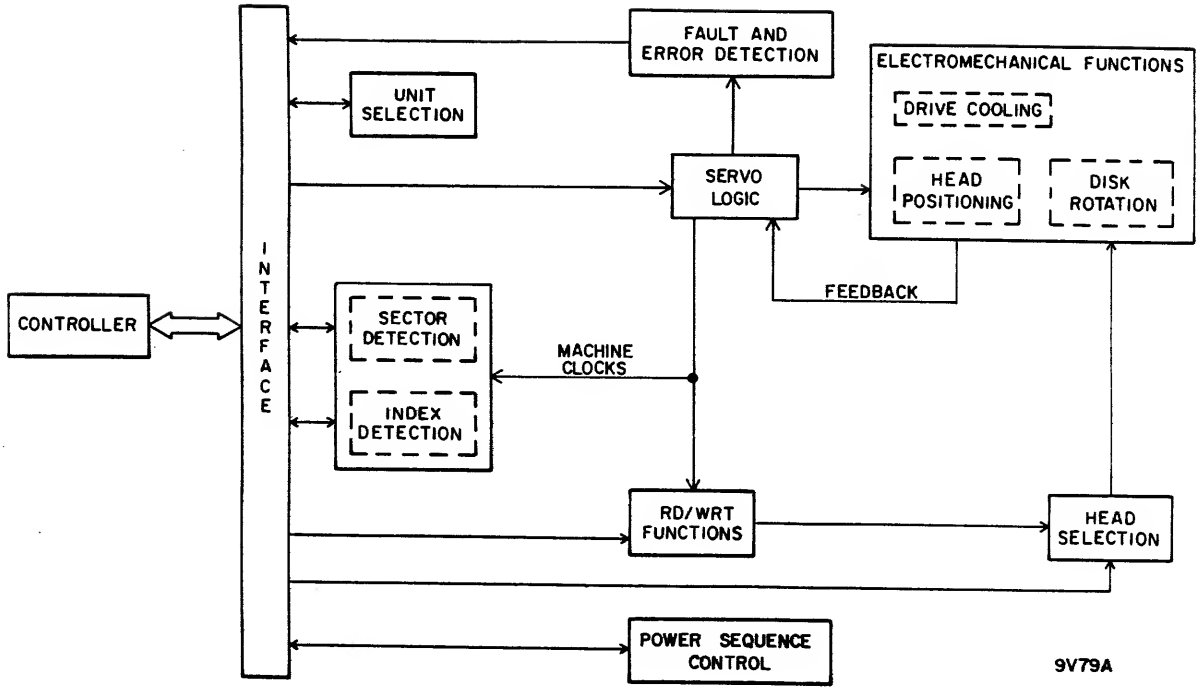

Figure 1-4. Block Diagram

the tag bus signals. In addition to the commands, the controller sends write data, write clock, and power sequence information to the drive. The drive sends various status signals to the controller via the device status lines. The drive also sends read data, read clock, and servo clock information to the controller. The controller uses these signals to monitor and control operations performed by the drive. Figure 1-5 shows all of the signal lines contained in the interface cables. The interface lines are described in section 3 of this manual.

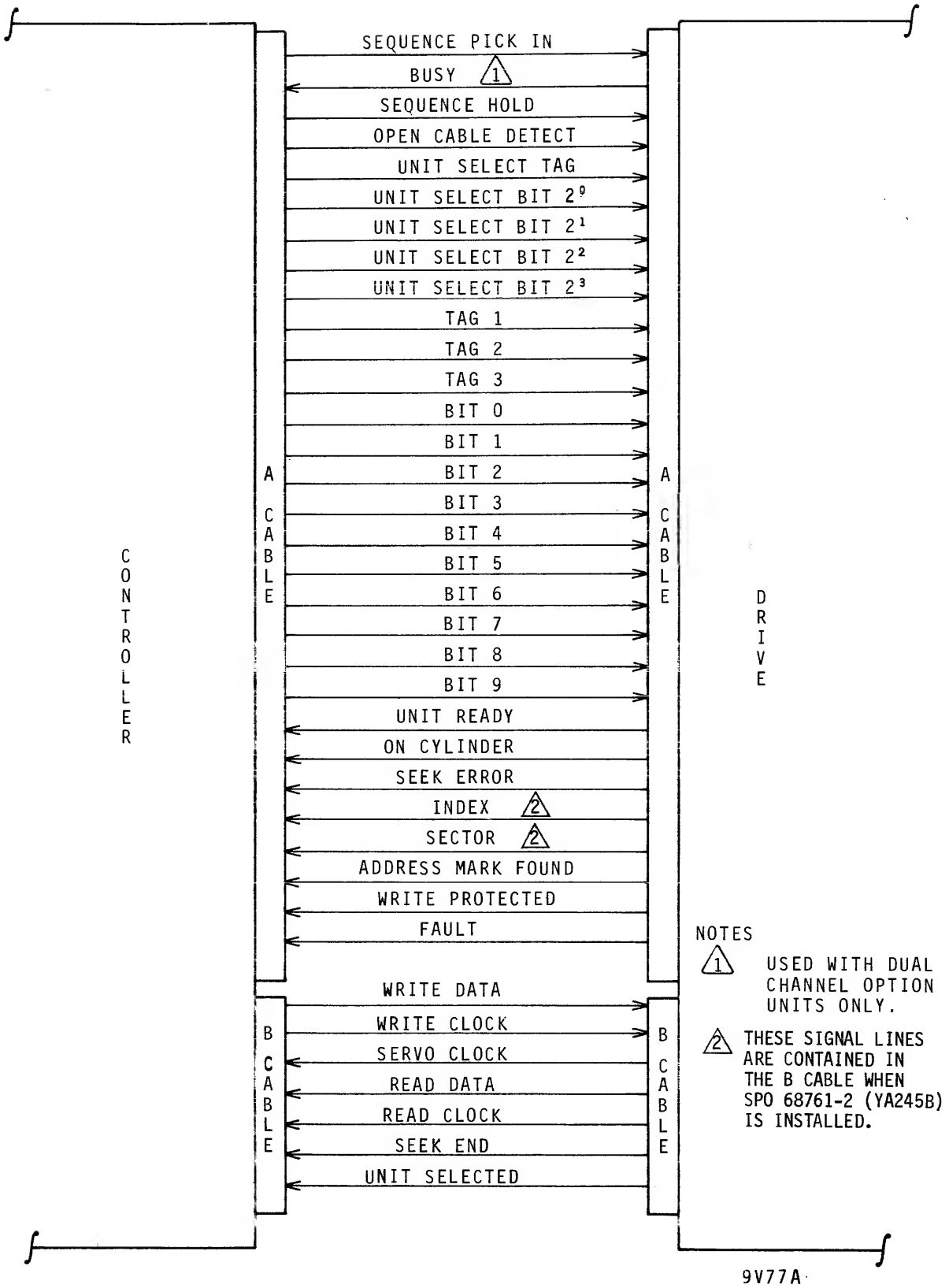

Figure 1-5. Interface Signal Lines

SECTION 2

OPERATION

INTRODUCTION

This section provides the information and instructions to operate the drive. It is divided into the following areas:

- Switches and indicators -- Locates and describes the various controls and indicators.
- Operating instructions -- Describes procedures for operating the drive.

SWITCHES AND INDICATORS

GENERAL

Switches and indicators are found in eight locations on the drive:

- Operator Panel
- Diagnostic Control Panel
- DC Power Supply
- AC Power Supply
- Dual Channel Steering Card (slot A07)
- MPU Test and Diagnostic Memory card (slot B03/C03)
- Fault/Control card (slot B04/C04)
- Drive Motor

The switches and indicators at all locations except the drive motor are shown in figures 2-1 and 2-2, and explained in the following text.

OPERATOR PANEL

The operator panel contains three switch/indicators and one indicator. These controls and indicators are described in table 2-1.

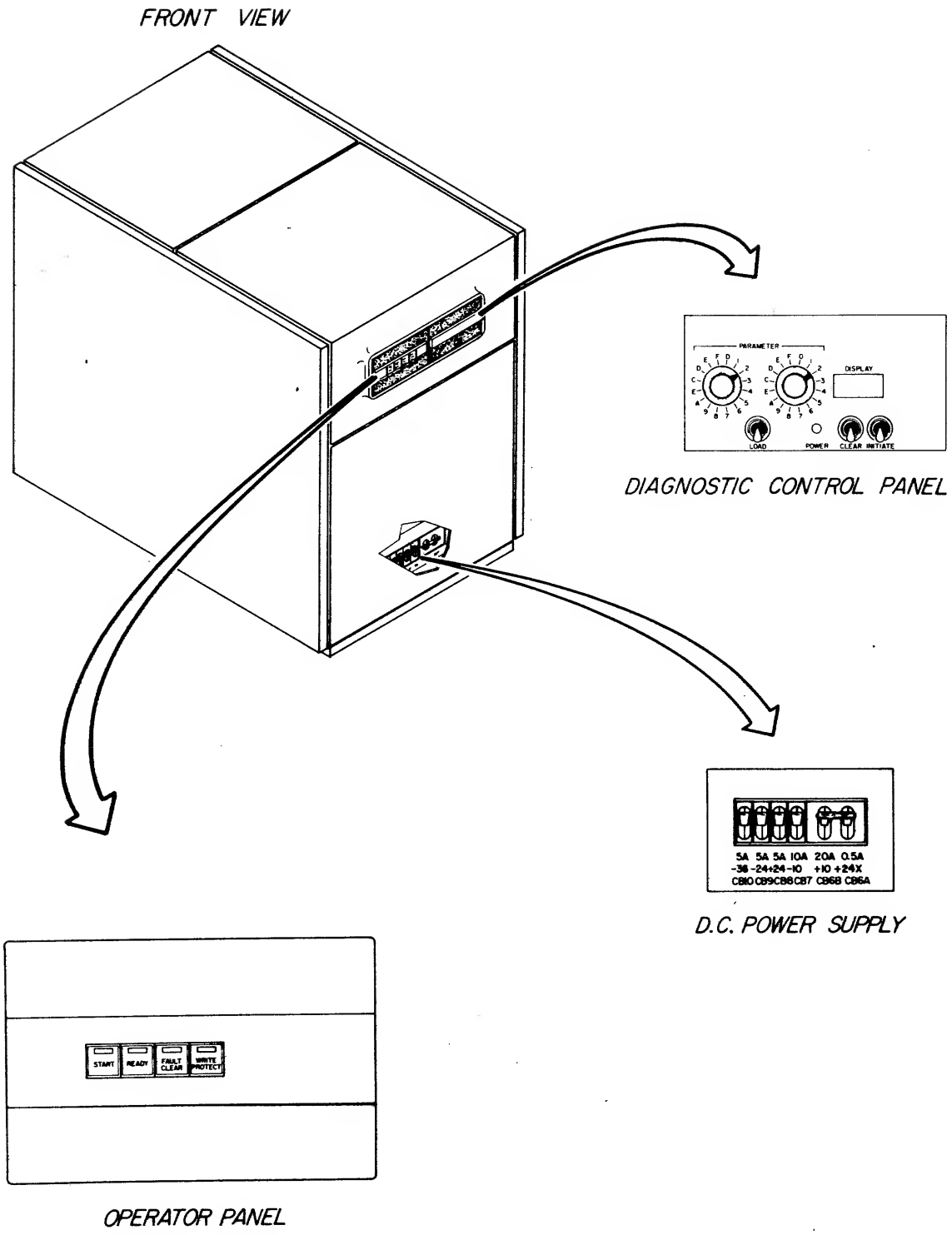

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Figure 2-1. Switches and Indicators (Front View)

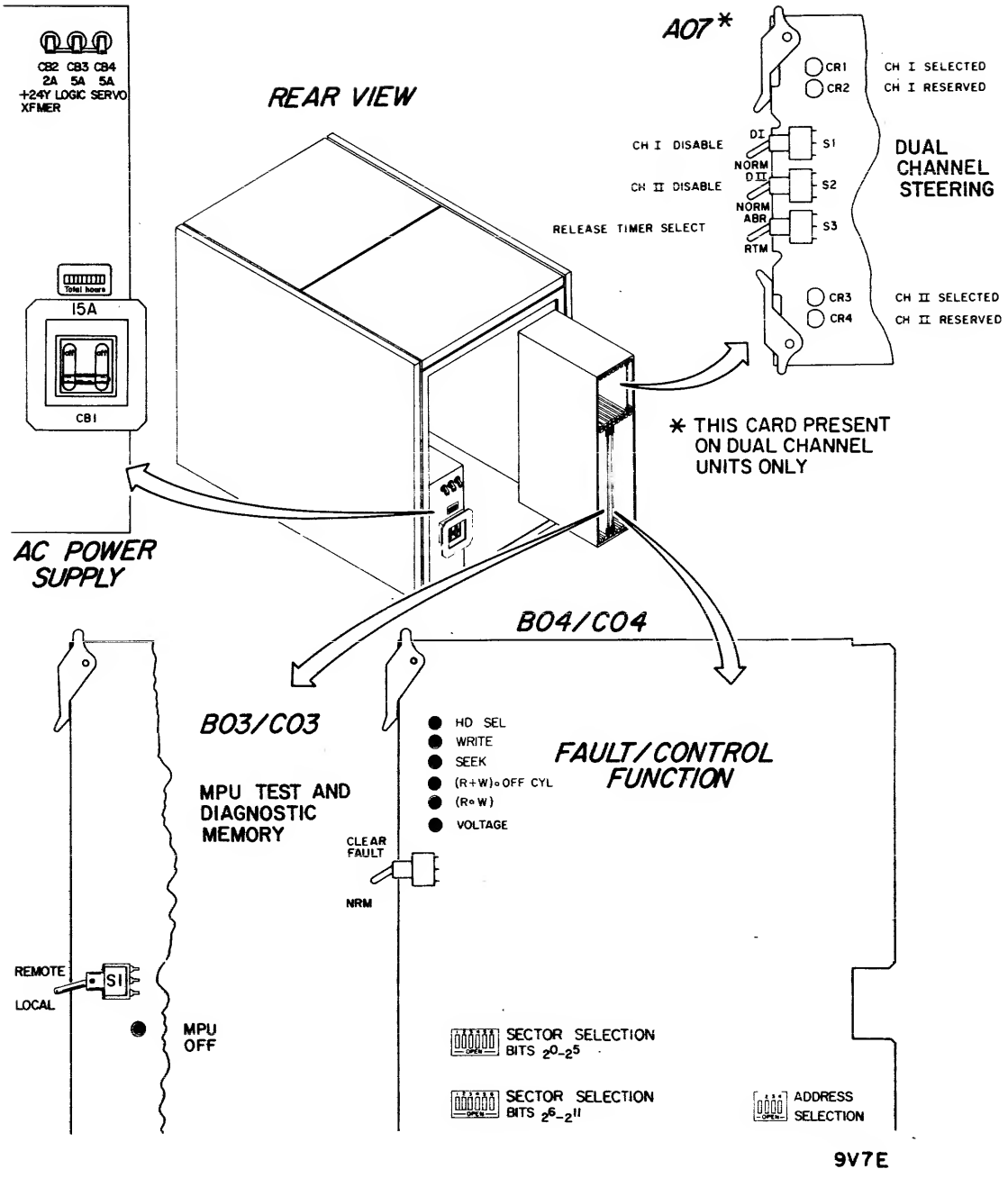


Figure 2-2. Switches and Indicators (Rear View)

TABLE 2-1. OPERATOR PANEL SWITCHES AND INDICATORS

Control/ Indicator	Function
START Switch/Indicator	Controls power application to drive spindle motor. Indicator is lit when switch is pressed. Pressing switch initiates spindle motor rotation and causes read/write heads to move to physical track zero after a 15-second timeout, provided the spindle motor is up to speed. Pressing switch again causes the spindle motor to stop and the read/write heads to move to Carriage Home position.
READY Indicator	Indicates that the drive is ready to receive and respond to commands from the controller.
FAULT CLEAR Switch/Indicator	Indicates that a fault condition exists within the drive. Refer to the trouble-shooting manual for a description of the fault conditions. The indicator is turned off by any of the following (provided the cause of the fault has been corrected): • Pressing the FAULT CLEAR switch on the operator panel. • Receiving a Fault Clear (Tag 3 with BOB 4) command from the controller. • A drive power-up operation • Activating the Clear Fault Switch on the Fault/Control card.
WRITE PROTECT Switch/Indicator	Pressing the switch (to light the indicator) disables all write operations. Pressing the switch again clears the WRITE PROTECT indicator and removes the drive from write protect mode.

DIAGNOSTIC CONTROL PANEL

The diagnostic control panel contains three toggle switches, two rotary switches, a power indicator, and a four-digit LED display. These controls and indicators are described in table 2-2.

TABLE 2-2. DIAGNOSTIC CONTROL PANEL SWITCHES AND INDICATORS

Control/ Indicator	Function
PARAMETER Switches	Sets up test numbers and parameters for entry into micro memory.
CLEAR Momentary Switch	Clears selected micro memory locations and terminates diagnostic activity.
INITIATE Momentary Switch	Initiates tests stored in micro memory.
POWER Indicator	Lights to indicate that the +5 V MPU power supply is supplying power to the _VWV card.
DISPLAY LED Indicators	Displays errors occuring during power up/ down sequencing, power supply failure, or as the result of servo or logic malfunction. The DISPLAY indicators also display the contents of selected micro memory locations when executing diagnostics.
LOAD Momentary Switch	Loads data from PARAMETER switches into micro memory.

DC POWER SUPPLY

The dc power supply circuit breakers control the application of -36 V, ±24 V, ±10 V and +24X power as described in table 2-3.

TABLE 2-3. DC POWER SUPPLY CIRCUIT BREAKERS

Circuit Breaker	Function
-36 V (CB10)	Controls -36 V to the servo power amplifier.
+24 V (CB9) -24 V (CB8)	Controls ±24 V to servo circuits and read/write circuits.
+10 V (CB6B) -10 V (CB7)	Controls ±10 V input to the ±5 V dc regulators supplying power to the backpanel and deck.
+24X V (CB6A)	Controls application of +24X V bias to the ±5 V regulators.

AC POWER SUPPLY

The ac power supply circuit breakers control the application of ac power to the input of the +24Y transformer in the ac power supply and protect the input to the ±10 V, ±24 V and -36 V transformers in the dc power supply. The application of ac power to the dc power supply is controlled by the test and diagnostic microprocessor. The TOTAL HOURS meter, located on the ac power supply, records continuously as long as the MAIN ac circuit breaker is on. Table 2-4 describes the function of each circuit breaker in the ac power supply.

TABLE 2-4. AC POWER SUPPLY CIRCUIT BREAKERS

Circuit Breaker	Function
MAIN (CB1)	Controls the application of all ac power input to the unit.
+24Y XFMER (CB2)	Controls the application of ac power to the +24Y and 5V MPU transformer that control the +5 V MPU power supply. +5 V MPU power is used to operate the operator/diagnostic panels and the test and diagnostic microprocessor at location B03/C03 in the logic chassis. +24Y power enables the operation of the drive motor and controls the application of ac power to the dc power supply.
LOGIC (CB3)	Protects the primary of the ±24 V and ±10 V transformers in the dc power supply.
SERVO (CB4)	Protects the primary of the -36 V transformer in the dc power supply.

DUAL CHANNEL STEERING CARD

The switches and indicators on the dual channel steering card are used to control and monitor the interface logic on units equipped with the dual access feature. Table 2-5 describes the controls and indicators on the card.

MPU TEST AND DIAGNOSTIC MEMORY CARD

The Local/Remote switch located on the MPU test and diagnostic memory card (slot B03/C03 in the logic chassis) is used to control power sequencing in the drive. When the switch is set to Remote (up position), drive power sequencing is enabled by a ground path from the controller (assuming the unit is connected to site power receptacle and MAIN circuit breaker CB1 is on). When the switch is set to Local (down position), sequence power

TABLE 2-5. DUAL CHANNEL STEERING CARD SWITCHES AND INDICATORS

Controls/ Indicators	Function
CH I SEL Indicator (CR1)	Lights to indicate that channel 1 is selected.
CH I RES Indicator (CR2)	Lights to indicate that channel 1 is reserved to the controller.
CH II SEL (CR3) Indicator	Lights to indicate that channel 2 is selected.
CH II RES (CR4) Indicator	Lights to indicate that channel 2 is reserved to the controller.
CH I Disable Switch (S1)	In the NRM position, this switch allows normal dual channel operation. In the DI position, it disables channel 1 for maintenance or prevents channel selection during normal operation.
CH II Disable Switch (S2)	In the NRM position, this switch allows normal dual channel operation. In the DII position, it disables channel 2 for maintenance or prevents channel selection during normal operation.
Release Timer Select Switch (S3)	Determines whether the drive will be in RTM (reserve timeout) mode or in ABR (absolute reserve) mode. If the switch is in the RTM position, the drive is released from reserved condition after 500 ms (nominal) of no channel activity. If switch is in ABR position, drive remains reserved until it receives either a release or priority select command.

is enabled as soon as the unit is connected to the site power receptacle (assuming all circuit breakers are ON). The START switch must be ON (lit) to enable spindle motor rotation regardless of the power sequencing mode. The MPU OFF indicator is lit whenever the microprocessor is not processing data.

FAULT/CONTROL CARD

Fault conditions are stored in six latches located on the fault/control card (slot B04/C04 in the logic chassis). A second group of latches stores selected fault conditions for display on the LED indicators located on the edge of the fault/control card. Table 2-6 describes the fault indicators. The fault latches can be cleared by performing one of the following operations:

a. Pressing the FAULT/CLEAR switch on the operator panel

b. Executing an RTZ seek (seek error only)

c. Executing a controller Fault Clear (Tag 03 with Bus Out Bit 4 active).

Clearing the fault latches does not turn off the indicators; they remain on for further maintenance action. The indicators can be turned off by performing one of the following operations:

a. Setting the PARAMETER switches on the diagnostic control panel to D0, and then pressing LOAD and INITIATE switches

b. Activating the Clear Fault switch located on the Fault/Control card.

The Sector Selection and Address Selection switches are also located on the fault/control card (see table 2-6). The Sector Selection switches allow the operator to establish a pattern of interrupts based on the angular position of the read/write heads with respect to index. A maximum of 128 segments (interrupts) can be selected. The rules for sector selection are described in the Installation and Checkout section of the Maintenance Manual Volume 1.

The Address Selection switches define the logical address of the unit. These switches allow the user to select addressing between hexadecimal 0 and F. Volume 1 also contains additional information on unit addressing.

DRIVE MOTOR THERMAL RESET SWITCH

The thermal reset switch is used to restart the drive motor following an overheat condition. The switch is located at the base of the motor adjacent to the brake.

OPERATING INSTRUCTIONS

POWER ON PROCEDURE

Local Mode

The following steps describe how power is applied to the drive when operating in Local mode, that is, when the Local/Remote switch is set to Local (switch in down position):

1. Set all circuit breakers to ON (power applied to all circuits except spindle motor, assuming no fault conditions are present).

2. Set START switch to ON (turns on spindle motor).

3. Assuming no fault conditions are present, disk comes up to speed and first seek (RTZ) occurs. READY indicator is lit at completion of first seek.

Remote Mode

The following steps describe how power is applied to the drive when operating in Remote mode, that is, when the Local Remote switch is in Remote (up position):

1. Set all circuit breakers to ON (power is applied to all circuits except the spindle motor, assuming sequence ground from the controller is active and no fault conditions are present).

2. Set START switch to ON (turn on spindle motor).

3. Assuming no fault conditions are present, disk comes up to speed and first seek (RTZ) occurs. READY indicator is lit at completion of first seek.

POWER OFF PROCEDURE

Local Mode

Either of the following operations causes the heads to retract and shuts off the spindle motor:

1. Set START switch to OFF.

2. Set MAIN circuit breaker to OFF (removes all power from unit).

TABLE 2-6. FAULT/CONTROL CARD SWITCHES/INDICATORS

Switch/Indicator	Meaning
Write Fault Indicator	Indicates nonexistent write current or failure to start writing within 4.0 µs after Write Gate is activated.
Head Select Fault Indicator	Indicates that two or more read/write heads are selected simultaneously.
Read or Write and Off Cylinder Fault Indicator	Indicates that the read/write heads have gone off cylinder during a read or write operation.
Read and Write Fault Indicator	Indicates that Write Gate and Read Gate are active simultaneously.
Seek Error Indicator	Indicates a seek error has occurred. Refer to the troubleshooting manual for a description of error codes associated with seek errors.
Sector Select Switches	Selects the number of sector interrupts desired by the user.
Address Selection Switches	Selects the unit logical address.
Voltage Fault Indicator	Indicates that one or more dc voltage is out of tolerance.
Clear Fault Switch	Used to clear the fault indicators and status latches on the fault/control card, and the CLEAR FAULT indicator on the operator panel.

Remote Mode

Any of the following operations causes the heads to retract and shuts off the spindle motor:

1. Set START switch to OFF.
2. Drop sequence ground from controller (removes power from dc power supply).
3. Set MAIN circuit breaker to OFF (removes all power from unit).

SECTION 3

THEORY OF OPERATION

THEORY OF OPERATION 3

INTRODUCTION

The theory of operation section describes the drive operations and hardware/controlware used in performing them. It is divided into the following major areas:

- Power Functions - Describes power distribution and sequencing.
- Electromechanical Functions - Provides a physical and functional description of the mechanical and electromechanical portions of the disk rotation, head positioning, and air flow systems.
- Interface - Describes the function of the signal lines connecting the drive to the controller.
- Unit Selection - Explains how the controller logically selects the drive so that the unit will respond to controller commands.
- Servo System - Describes how the servo system controls read/write head movement over the disk surface; how the servo system derives the machine clocks used by the sector, guardband, index, and read/write circuits.
- Guardband and Index Detection - Describes how the drive detects the guardbands that indicate whether the heads are outside the legal recording areas, and the index pattern that is used to indicate the logical beginning of each track.
- Sector Detection - Explains how the drive derives the sector pulses that are used to determine the angular position, with respect to index, of the read/write heads.
- Head Selection - Explains the head selection process.
- Read/Write Functions - Describes how the drive processes the data that it reads from, or writes on, the disk.
- FTU Functions - Describes the operation of the resident Field Test Unit.

The descriptions in this section are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software.

Functional descriptions are frequently accompanied by block diagrams or simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. These diagrams are not updated as frequently as the logic diagrams in the maintenance manual. Therefore, the diagrams (and timing generated from them) in the hardware maintenance manual should take precedence over those in this manual if there is a conflict between the two.

NOTE

Numbers appearing in parentheses in this manual are cross references to the logic diagrams in the maintenance manual.

POWER FUNCTIONS

GENERAL

The drive power supply receives its input from the site ac power source and uses it to produce the dc voltages necessary for drive operation. Power from the site is made available to the drive via the MAIN ac circuit breaker (A1BCB1) located on the ac power supply. Power functions may be grouped into two major categories:

- Power Distribution - How power is distributed to the drive circuitry.
- Power Sequencing - How power is applied to, and removed from, the drive circuitry.

POWER DISTRIBUTION

Site power is distributed to the drive circuits as shown in figure 3-1, sheets 1 and 2. All circuits are protected by circuit breakers located in the ac and dc power supplies. All dc voltages are automatically checked at the input to each load. Voltage levels at the load can be checked by tests executed from the diagnostic panel.

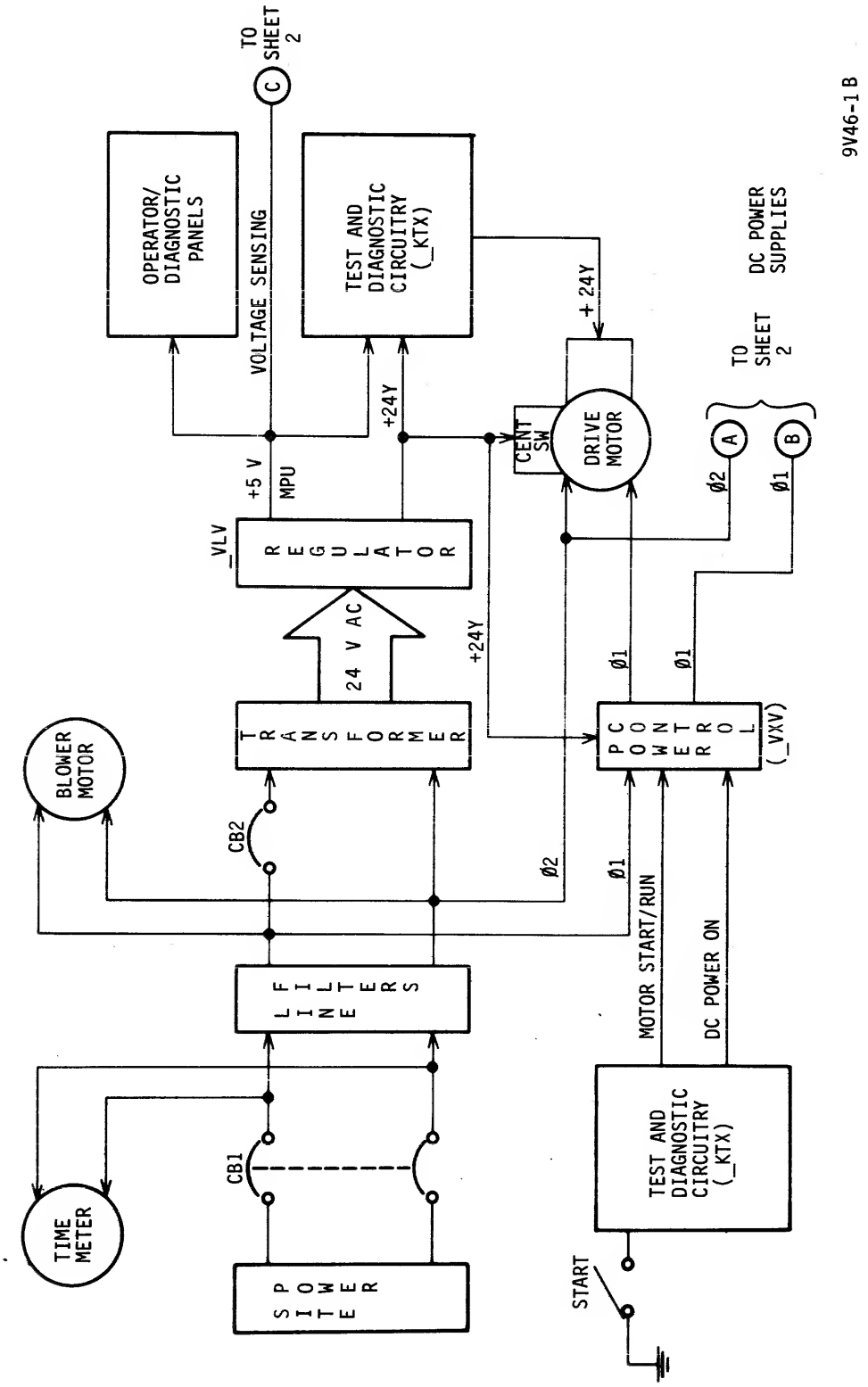


Figure 3-1. Power Distribution (Sheet 1 of 2)

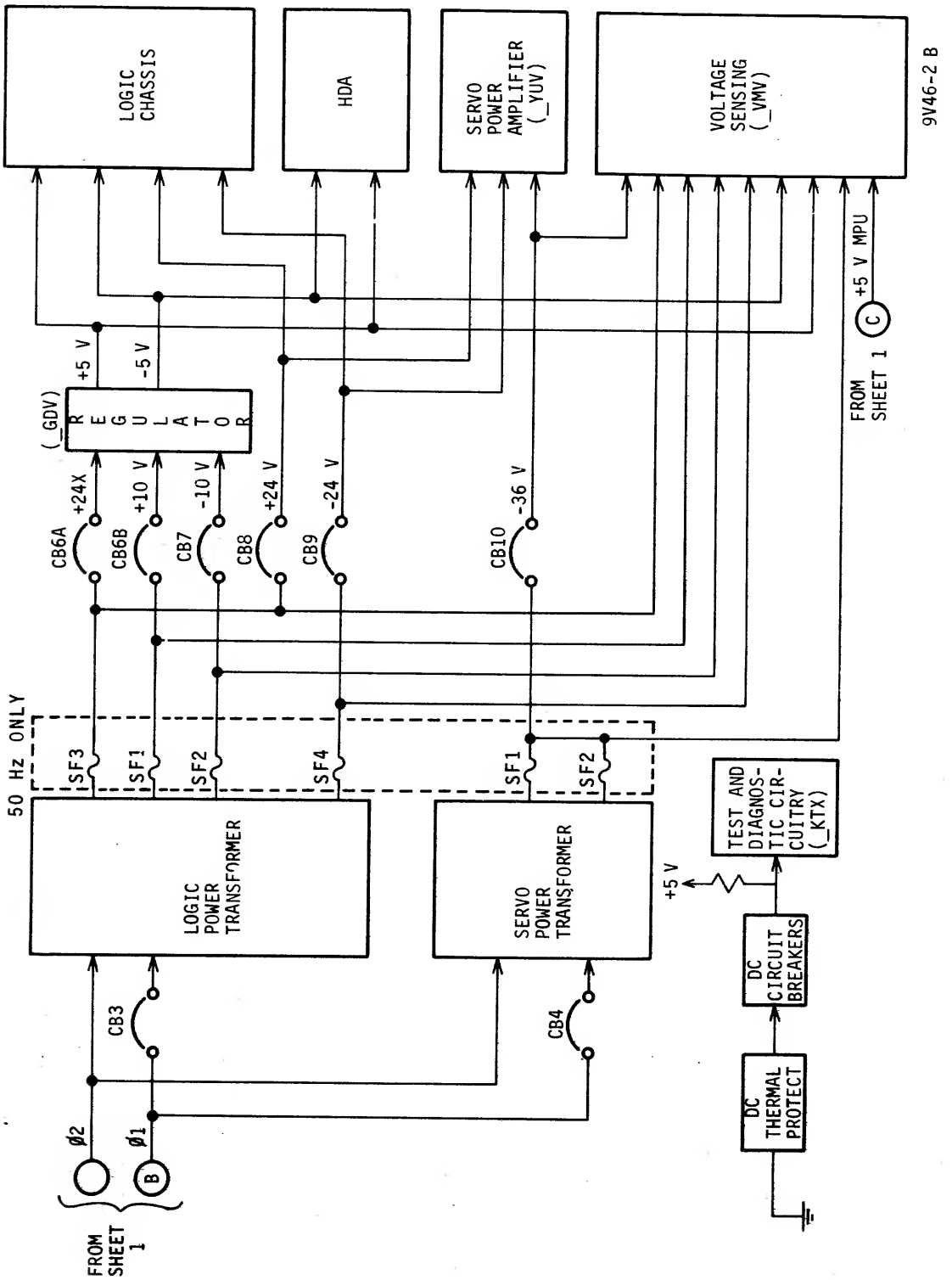


Figure 3-1. Power Distribution (Sheet 2)

POWER SEQUENCING

Power on/off sequencing is performed by the logic shown in figure 3-2. It is controlled by the microprocessor located on the _KTX card (slot B03/C03 in the logic chassis).

ELECTROMECHANICAL FUNCTIONS

DRIVE MOTOR

The drive motor rotates the disks in the HDA. A belt and pulley arrangement (figure 3-3) transfers motion to the HDA disks. The motor mounts on a movable plate that attaches to the deck casting. Springs connected between the motor mounting plate and deck casting maintain the tension required to keep the belt tight.

BRAKE

The brake mounts on the bottom of the motor. Its purpose is to stop the motor within 15 seconds of the start of the power off sequence.

The brake consists of an electromagnet and a clutch mechanism as shown in figure 3-3. The motor shaft passes through the center of the electromagnet and couples to the friction part of the clutch.

The electromagnet is energized at the start of a power up sequence. Energizing the electromagnet pulls the upper clutch plate away from the motor shaft, allowing the friction disk to rotate freely.

During the power-off sequence, the microprogram deenergizes the electromagnet at the same time as the motor. With the electromagnet deenergized, the upper braking springs push the upper clutch plate downward, squeezing the friction disk between the upper and lower clutch plates. Because the friction disk couples directly to the motor shaft, the resulting drag on the friction plate causes the motor to decelerate.

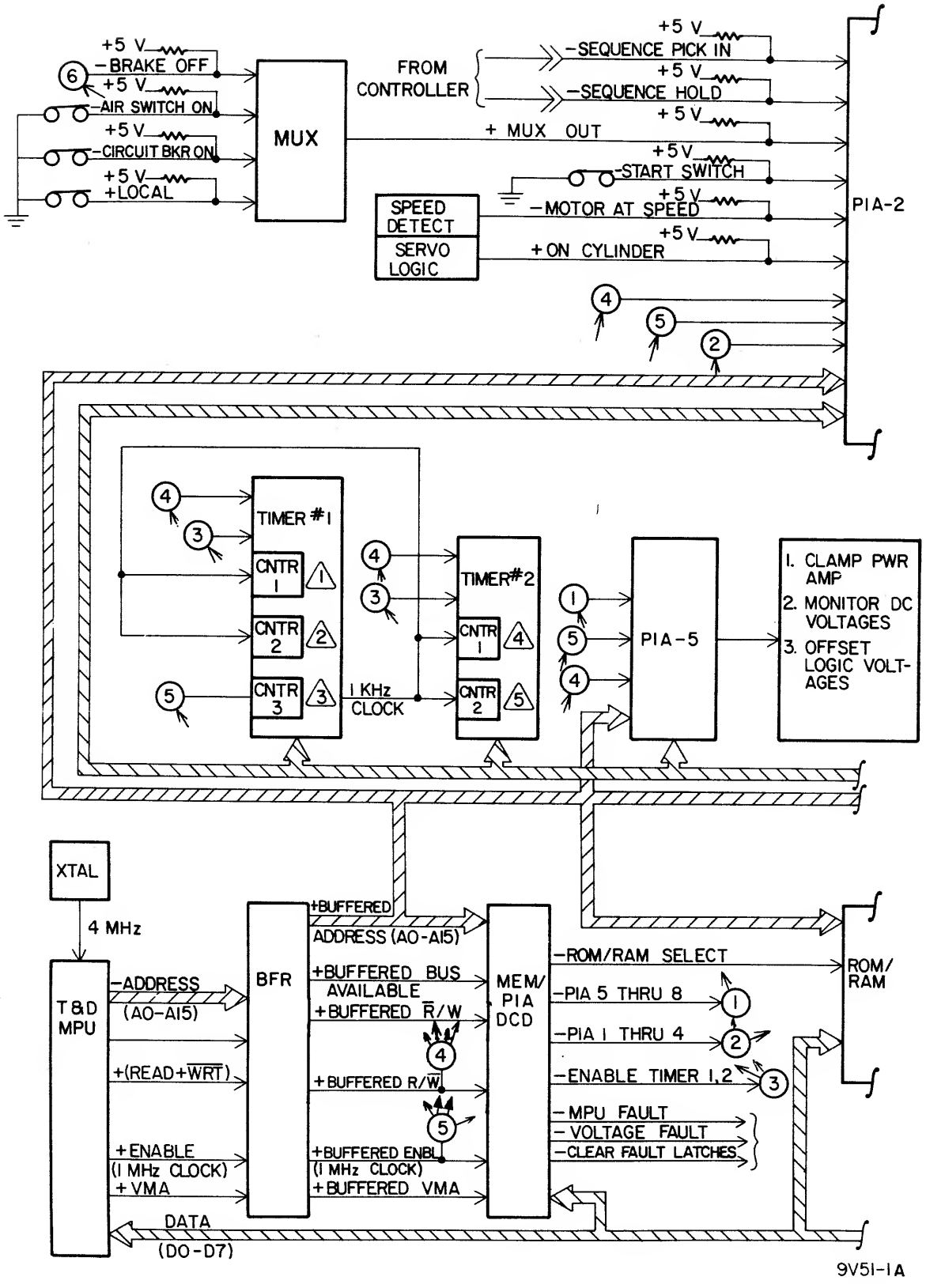


Figure 3-2. Power Sequencing Logic (Sheet 1 of 2)

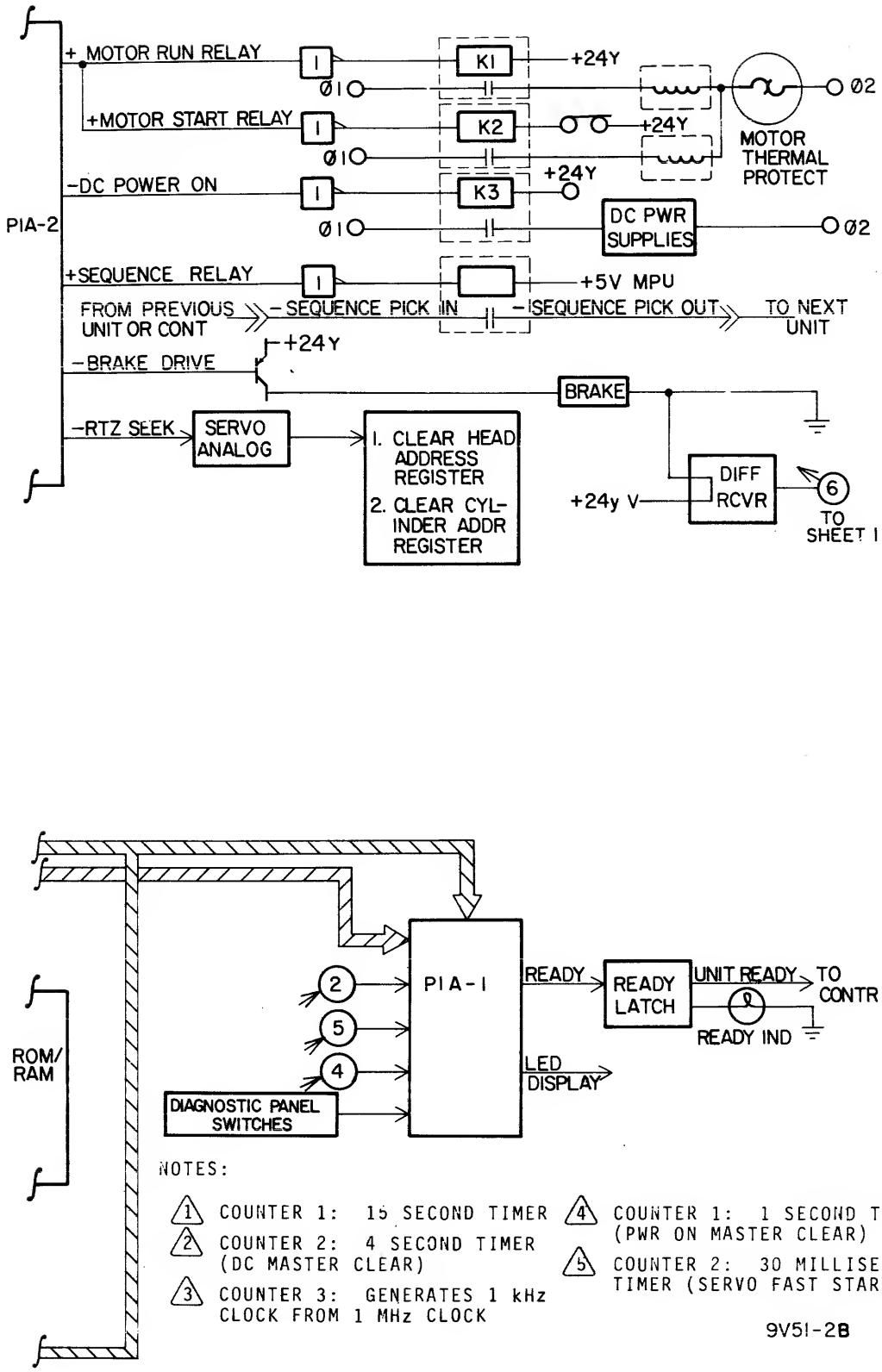


Figure 3-2. Power Sequencing Logic (Sheet 2)

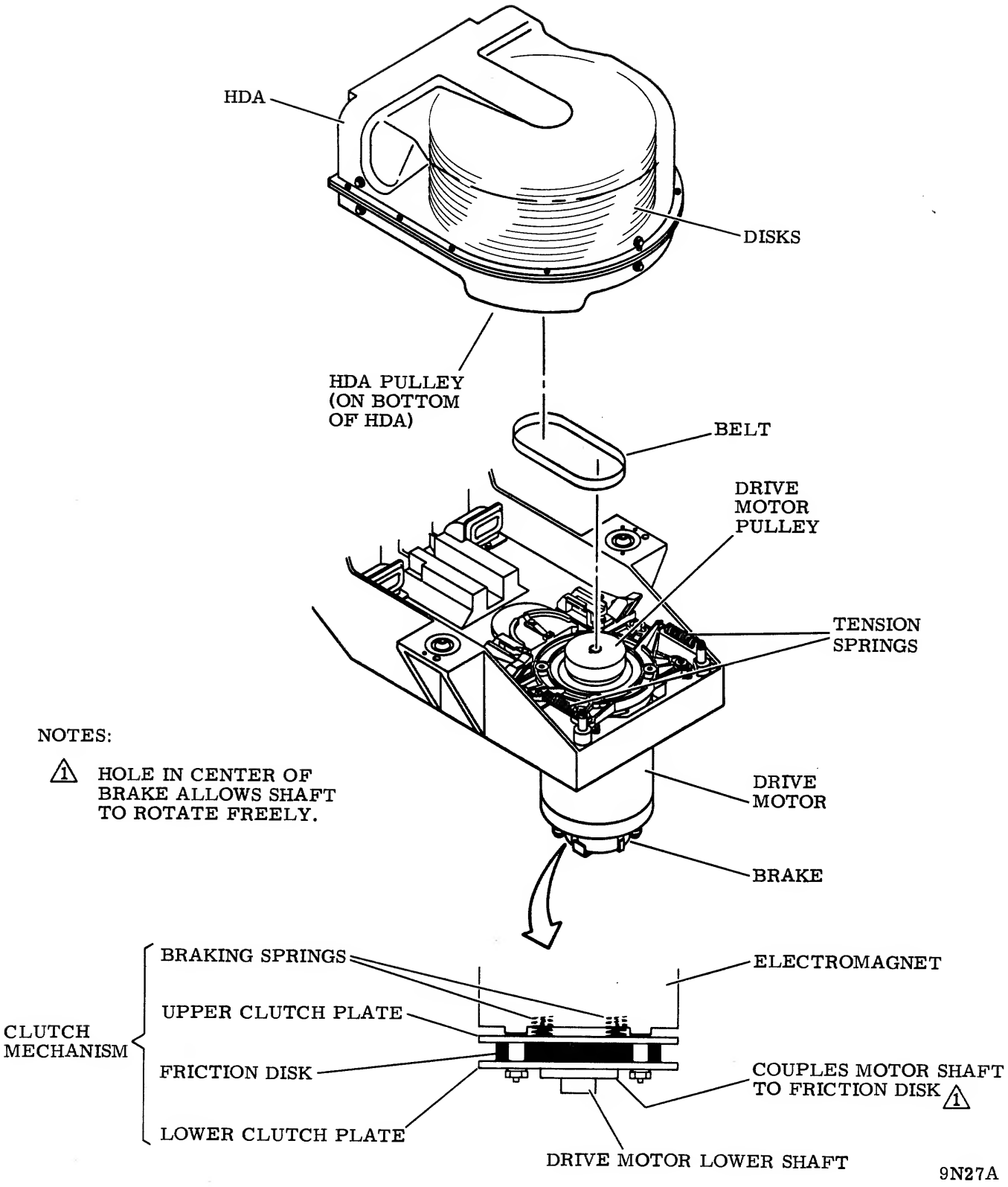


Figure 3-3. Disk Rotation Mechanism

INITIAL SEEK

If operating in local mode, pressing the START switch on the operator panel releases the drive motor brake and allows the drive motor to come up to speed provided dc power is active and functioning normally.

If operating in remote mode, all of the following conditions must be present to release the drive motor brake and cause the drive motor to come up to speed:

a. START switch must be enabled (on).

b. Pick and Hold signals from the controller or previous drive must be active.

c. DC power supply must be active and functioning normally.

The drive performs an initial seek (RTZ) at the conclusion of a 15-second timeout after START switch is pressed, provided the motor is up to speed. At the completion of the first seek, the drive is ready for operation. See figure 3-4.

During a power-off sequence, the heads move to the carriage home position, power is removed from the drive motor, and the brake halts disk rotation within 15 seconds. Power-off sequencing can be initiated by any of the following conditions:

a. Pressing the START switch a second time.

b. Pick and Hold signals inactive if operating in Remote mode.

c. A Retract Fault occurs.

RETRACT FAULT CONDITIONS

The following conditions cause the read/write heads to retract and the drive motor to stop:

- Loss of ac power
- Loss of +24Y or +5 V MPU power
- Loss of speed -- spindle motor speed has dropped below 3000 revolutions per minute
- Drive motor thermal overload -- overheat condition within the drive motor
- Blower failure -- loss of cooling air at the input to the HDA

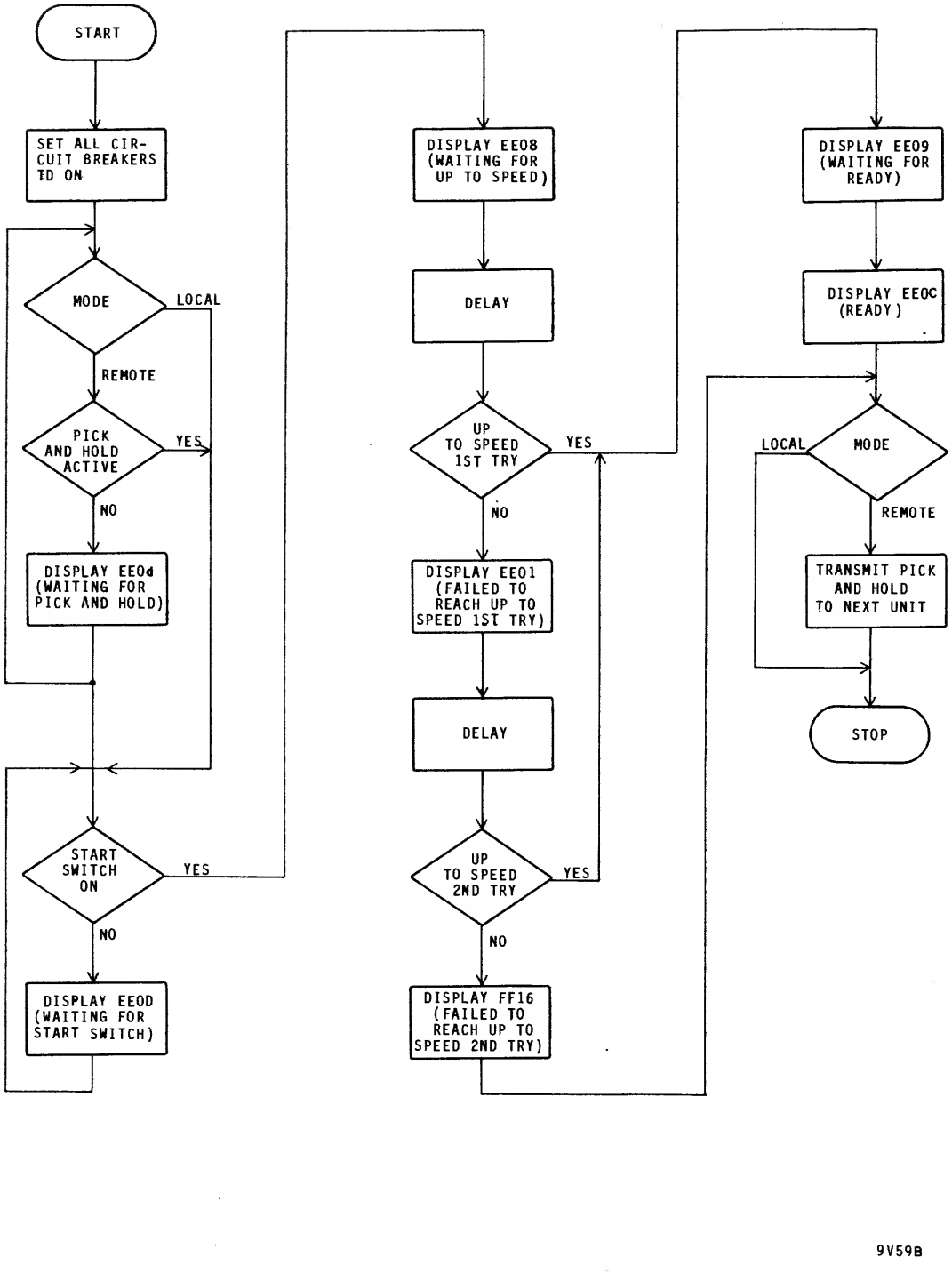


Figure 3-4. Power Sequencing Flowchart

- Any circuit breaker open.
- Failure of any dc voltage to remain within tolerance.

VENTILATION AND COOLING

Two separate air flow systems are used for cooling: a high-pressure system and a low-pressure system. Both systems are driven by a common blower motor configured with two impellers. Both impellers are mounted in the same metal housing. See figure 3-5.

Input air for both systems enters the plenum located underneath the front of the cabinet. Air entering this port passes through a coarse filter that prevents entry of large particles into the system. Input air is ducted through the plenum to the blower assembly.

High-Pressure System

The high-pressure system cools and ventilates the HDA. The high-pressure blower (narrower of the two impellers) forces air through the absolute filter, through the HDA, past the magnet assembly, and out the muffler assembly of the HDA into the lower part of the cabinet. A pressure switch is located in the filter housing leading to the HDA. If the air pressure falls below a safe level, the power-on sequence logic turns off the drive motor and causes a retract operation.

Low-Pressure System

The low-pressure system cools and ventilates the dc power supply and the logic chassis. Air is vented through the top of each assembly. The dc power supply contains a thermal breaker that can shut down all voltages produced by the dc power supply if the temperature exceeds 135° C (275° F).

INTERFACE

I/O CABLES

The interface is provided by two cables for a single-channel unit and by four cables for a dual-channel unit.

The "A" cable for each channel contains signal lines that carry commands and control information to the drive, and status information to the controller.

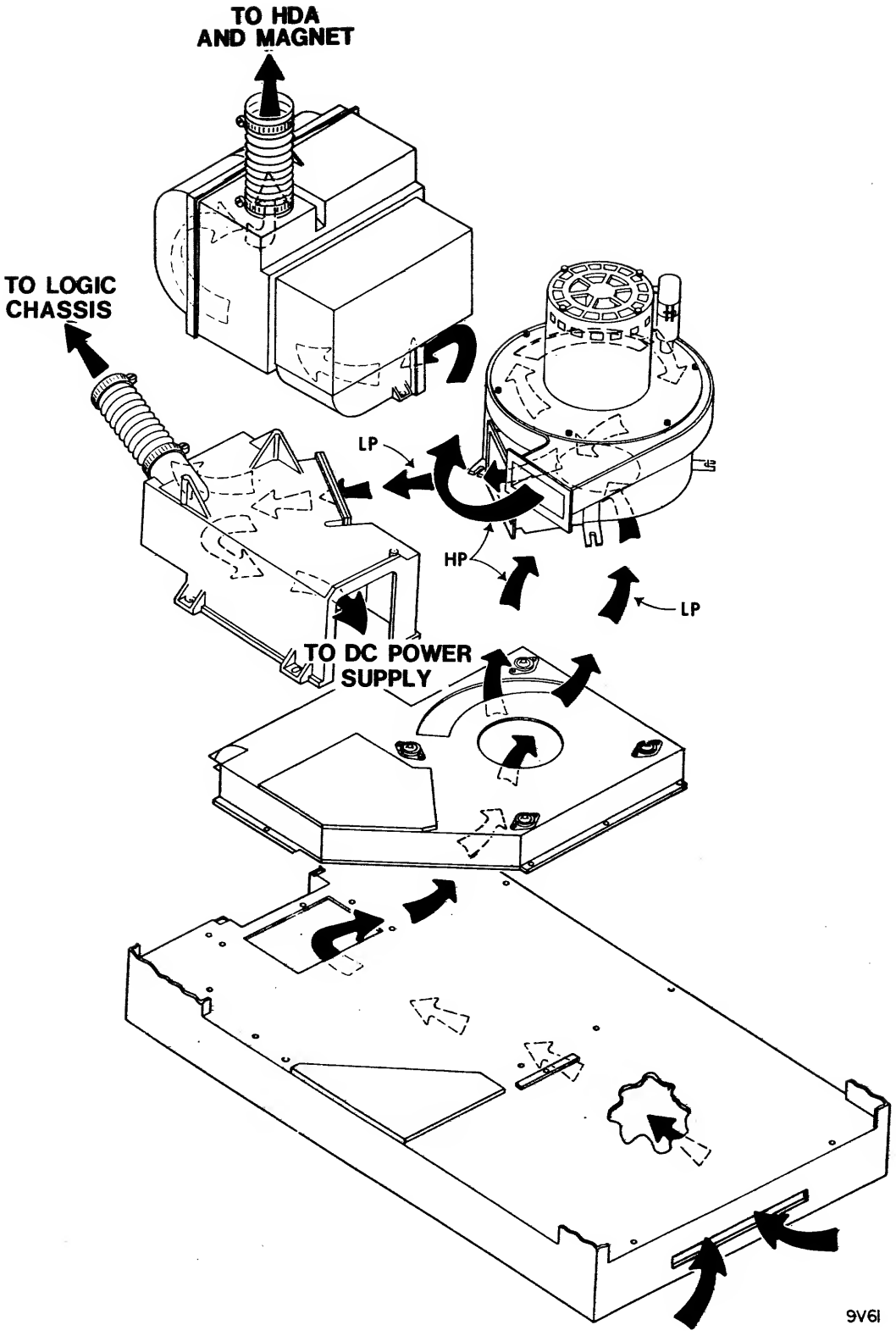


Figure 3-5. Ventilation

The "B" cable for each channel contains signal lines that carry read/write data, clock, and status information between the drive and controller.

An option is available that places the Index and Sector control signals on the "B" cable.

The "A" and "B" cables are either flat (60-pin) or round (75-pin), depending upon the drive model. Refer to the configuration chart in the Preface of this manual.

SIGNAL PROCESSING

All operations except local mode power-on are controlled from the controller. See figure 3-6.

Power must be applied to the drive before it can be selected. If operating in Remote mode (Local/Remote switch set to Remote position), Pick and Hold signals from the controller must be present to power up the unit. If the unit is selected and a first seek operation has been completed (Ready condition) the controller may execute commands that position the read/write heads over the desired cylinder, select the read/write head to be used, and initiate the read or write operation.

During a write operation, the drive receives data from the controller and writes it on the disk. During a read operation, the drive recovers data from the disk and transmits it to the controller.

Status information resulting from each drive operation is continuously transmitted to the controller as long as the drive is selected.

Table 3-1 lists and describes the signal lines connected between the controller and the drive.

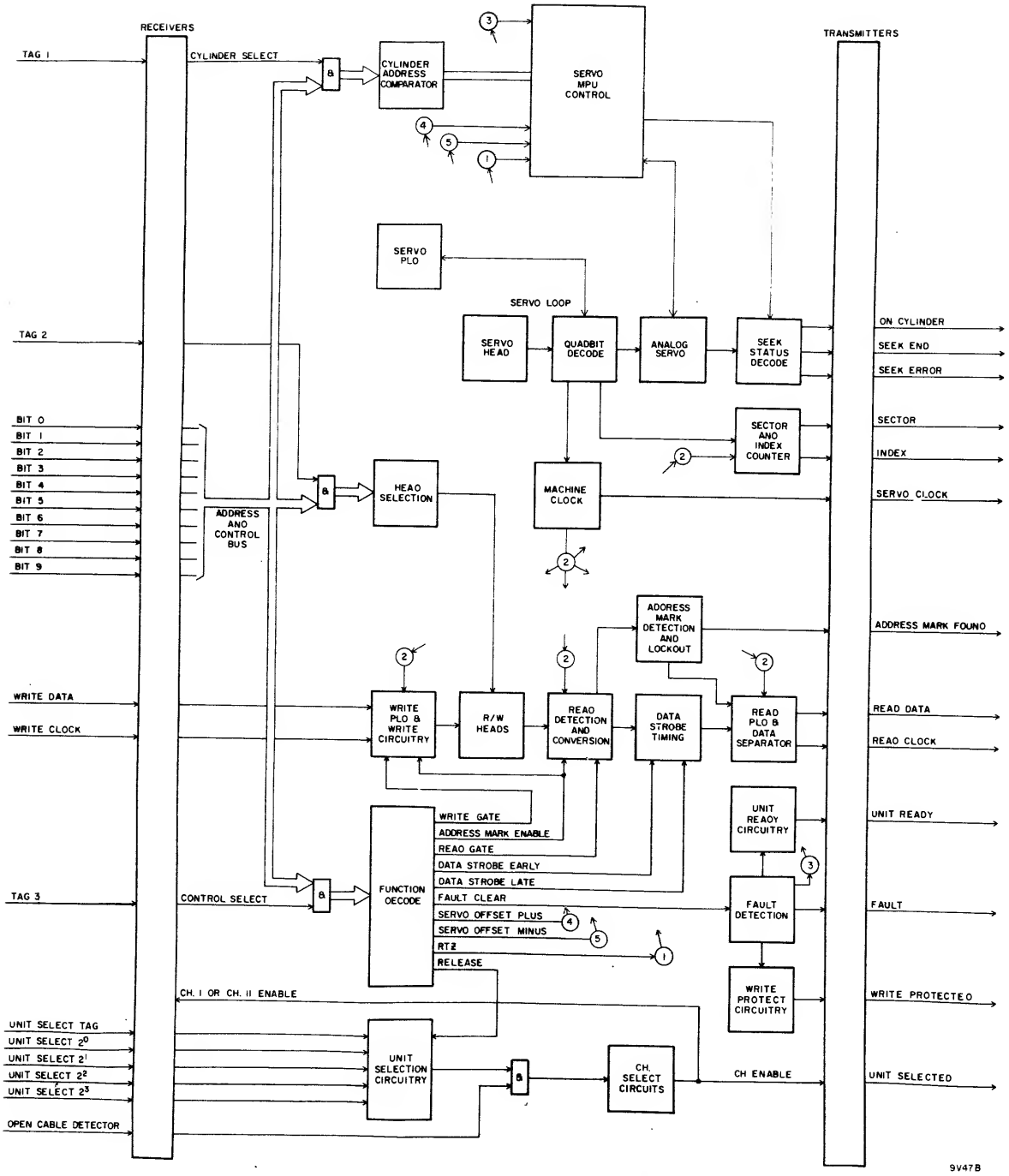


Figure 3-6. Signal Processing Block Diagram

TABLE 3-1. INTERFACE LINES

Signal	Meaning
Function: Power Up Sequencing	
Sequence Pick In	A ground from the controller on this line starts the power on cycle when the drive's Local/Remote switch is in the Remote (up) position.
Sequence Hold	A ground from the controller on this line holds the drives in a power on condition provided the START switch is on when operating the drive in the Remote mode (Local/Remote switch in the Remote position). Removing the ground from this line and from the Sequence Pick In line powers down all operating drives in the system.
Sequence Pick Out	When drives are connected in a daisy chain manner, the previous drive must be up to speed before the subsequent drive is activated. When the drive is up to speed, the Sequence relay is deenergized and the -Sequence Pick In signal is sent, via normally closed contacts of the Sequence relay, to the next drive. (Note: this signal is called -Sequence Pick Out when used as an output from the drive, but is called -Sequence Pick In when used as an input to the next drive).
Table Continued on Next Page	

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning
Function: Controller Selecting Drive	
Unit Select Tag	This signal gates Unit Select Bit lines into logical number compare circuit. Unit is selected after 600 nanoseconds (maximum) internal time lapse. Drive will not process commands until selected. When the Unit Select Tag is accompanied by a Bus Bit 9 active, this indicates a priority select status. The drive is unconditionally selected and reserved by the channel issuing this command provided that both channels are enabled and a priority select condition does not exist on the other channel. In dual-channel units, selection also causes the device to be reserved to the selecting channel. The reserve condition is cancelled by one of the following: 1. Executing a Release command 2. At the completion of the current operation provided the Release Timer Select switch on the card in slot A07 is set to RTM.
Table Continued on Next Page	

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning
	3. Executing a priority select from the other channel.
Unit Select Bits 2^0,2^1, 2^2, and 2^3	A binary code is placed on these four lines to select a drive. The binary code must match the logical address of the drive defined by the position of four switches on the card in slot B04/C04 of the logic chassis. Drives can be numbered 0 through 15.
Unit Selected	This signal indicates the drive has accepted a Unit Select request. This line must be active before the drive will respond to any command from controller.
Open Cable Detector	A voltage is supplied by the controller to override the bias voltage at drive receiver. If cable is disconnected or if controller power is lost, unit selection and controller commands are inhibited.
Function: Drive Indicates Operational Status	
Unit Ready	Unit Ready indicates that the drive spindle motor is up to speed, that the servo head is positioned on cylinder, and that no fault condition exists.

Table Continued on Next Page

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning
Index	This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero.
Sector	This signal is derived from the servo tracks and is used to indicate the beginning of each sector on the track. The number of sector signals that occur for each revolution of the disk is switch selectable on the card at location B04/C04 in the logic chassis.
Busy	This signal is generated when a controller attempts to select or reserve a drive that has already been selected and/or reserved by the other controller. This signal is sent to the controller attempting the selection.
Write Protected	When this line is high, it indicates that the drive write circuits are disabled. The write protect mode is enabled by the WRITE PROTECT pushbutton switch on the operator panel, or a fault condition. Attempting to write while the write protect mode is active results in a fault condition.
On Cylinder	This indicates that the servo head is positioned at a track. Any positioner movement, including servo offset, results in a loss of the signal. When operating in offset mode, this line drops momentarily, but comes back on after a delay.

Table Continued on Next Page

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning
	On Cylinder status is cleared by any seek instruction including a zero track seek.
Function: Controller Sends Commmands to Drive	
Bits 0 through 9 (Bus Lines)	These ten lines carry data to the drive. The meaning of the data is a function of the active tag line.
Tag 1 (Cylinder Select)	This tag line gates the data on the bus out lines to the drive Cylinder Address register. The bus bits have the significance listed below.

Bus Out Bit	Cyl Address Value	Fixed Head Function
0	1	Moving head cylinders are numbered from 000 thru 842. Fixed head cylinders are numbered from 896 thru 898.
1	2	
2	4	
3	8	
4	16	
5	32	
6	64	
7	128	
8	256	
9	512	

Tag 2 (Head Select)	This tag line gates the data on the bus lines to the drive Head Address register. The bus bits have the
Table Continued on Next Page	

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning
	significance listed below. Note that the bus bit functions are discussed for both the movable and fixed head select operations. Bus Out Bit / Head Address Value 0 / 1 1 / 2 2 / 4 3 / 8 4 / 16 5 / 32 Movable heads 00 through 39 may be selected in cylinders 000 thru 842. Fixed heads 00 through 39 may be selected in cylinder 896, fixed heads 40 through 79 in cylinder 897, and fixed heads 80 through 95 in cylinder 898.
Tag 3 (Control Select)	This tag line gates the data on the bus lines to the logic circuits of the drive for commanding various operations. The operation performed is dependent upon which of the bus lines is active. The significance of the bus bits is as follows:
Table Continued on Next Page	

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning		
	Bus Bit	Name	Function Performed
	0	Write Gate	Enables write driver. Operation not completed if a fault condition exists.
	1	Read Gate	Enables read circuitry. Leading edge triggers the read chain circuit to synchronize on an all-zeros pattern. Operation not completed if a fault condition exists.
	2	Servo Offset Plus	Causes the actuator to offset 100 microinches in the positive direction (toward the spindle) from the nominal On Cylinder position. Write operations cannot be performed in offset mode.
	3	Servo Offset Minus	Causes the actuator to offset 100 microinches in the negative direction (away from the spindle) from the

Table Continued on Next Page

TABLE 3-1. INTERFACE LINES (Contd)

Signal			Meaning
			nominal on cylinder position. Write operations cannot be performed in the offset mode.
	4	Fault Clear	Clears the fault latches provided fault condition no longer exists.
	5	Address Mark Enable	Writes an address mark when concurrent with Write Gate, or initiates an address mark search when concurrent with Read Gate.
	6	RTZ	Causes the drive to move the positioner to cylinder zero, track zero. It also resets the Head Address register and Seek Error latch.
	7	Data Strobe Early	Data Strobe Enables the PLO Early data separator to strobe the data at a time earlier than nominal.

Table Continued on Next Page

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning		
	8	Data Strobe Late	Enables the PLO data separator to strobe the data at a time later than nominal.
	9	Release (Dual Channel Option Only)	Clears channel reserved and channel priority select reserve status. (Refer to Unit Selection discussion.)
Function: Drive Response to Controller Command			
On Cylinder	Described previously.		
Seek End	This signal indicates either an on cylinder status or seek error status resulting from a seek operation that has terminated.		
Fault	When the line is active it indicates that one or more of the following faults exist: 1. Head Select Fault -- two or more heads selected simultaneously. Condition is cleared by the selection of only one head. Refer to description of Fault/Control card in section 2 to determine how to clear fault status and indication.		

Table Continued on Next Page

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning
	2. Write Fault -- Absence of write current, failure to detect write data within 4 microseconds after Write Gate, faulty head coil, or drive is in write protected mode. Condition is cleared by correcting the cause of the fault. Refer to description of Fault/Control card in section 2 to determine how to clear fault status and indication. 3. Off Cylinder and Read or Write Fault -- write or read attempted while off cylinder. Condition is cleared by dropping Read Gate or Write Gate. Refer to description of Fault/Control card in section 2 to determine how to clear fault status and indicator. 4. Read/Write Fault -- Read Gate and Write Gate are active simultaneously. Condition is cleared by dropping Read Gate or Write Gate. Refer to description of Fault/-Control card in section 2 to determine how to clear fault status and indication. 5. VOLTAGE FAULT -- one or more dc voltages are out of tolerance. Condition is cleared by correcting the cause of the fault. Refer to description of Fault/Control card in section 2 to determine how to clear fault status and indication.
Table Continued on Next Page	

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning
	6. Gated MPU Fault -- All conditions that cause 'FFxx' error codes in the test and diagnostic MPU. Condition is cleared by correcting the cause of the fault. Refer to description of Fault/-Control card in section 2 to determine how to clear fault status. Refer to the Troubleshooting Manual for a description of Gated MPU Fault error codes.
Seek Error	Generated by the Servo Logic upon detection of any of the following conditions: • Seek not completed within 500 milliseconds. • Guardband detected during normal seek. • No track crossings detected after seek start, except zero track length seek.
Table Continued on Next Page	

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning
	• Three or more track crossings during settle-in. • Too long to recover from overshoot during settle-in • Too much time to return to On Track following overshoot. • Failure to detect On Track during settle-in. • Servo head drifted off track during track following. • Seek to cylinder address beyond 842 except cylinders 896, 897 and 898. • Movable head selection beyond head 39 on cylinders 000 through 842. • Fixed head selection beyond head 39 on cylinder 896. • Fixed head selection outside the range from 40 through 79 on cylinder 897. • Fixed head selection outside the range from 80 through 95 on cylinder 898.
Table Continued on Next Page	

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning
	Condition is cleared by correcting the cause of the fault. Refer to description of Fault/Control card in section 2 to determine how to clear fault status and indication.
Address Mark Found	When an address mark has been found, this line goes high.
Functions: Read, Write and Clock	
Read Data	This line transmits data recovered from disk. This data is transmitted in NRZ form to the controller.
Read Clock	Read Clock defines the beginning of a data cell during a Read operation. This clock is derived from, and is synchronous with, Read data.
Write Data	This line transmits NRZ data from the controller to the drive for recording on the disk surface in MFM form.
Table Continued on Next Page	

TABLE 3-1. INTERFACE LINES (Contd)

Signal	Meaning
Write Clock	The 9.67 MHz Write Clock defines the beginning of a data cell during a Write operation. It is derived from the Servo Clock.
Servo Clock	Servo Clock is a phase-locked 9.67 MHz signal derived from the servo track quadbits. Servo Clock is transmitted to the controller and is used to generate Write Clock.

UNIT SELECTION

GENERAL

The drive must be selected before it will respond to any commands from the controller. This is the case because the tag and bus bit receivers, as well as certain transmitters, are not enabled until the drive is selected.

In both single and dual channel units, the select sequence is initiated by a Unit Select Tag signal from the controller. However, the sequence performed is different depending upon whether a single or dual channel is being considered. Since only one controller can communicate with the drive at a time, dual channel logic must solve the problem of priority when more than one controller wants to select the drive at the same time. The following paragraphs describe both single and dual channel selection.

SINGLE CHANNEL UNIT SELECTION

The single channel unit select sequence (see figure 3-7) starts when the controller sends the Unit Select Tag accompanied by a logical address on the four Unit Select lines.

The controller selects the drive by activating the Unit Select tag and placing an address on the Unit Select lines. If the address matches the setting of the Address Select switch on the card at B04/C04, an address compare occurs. If an address compare occurs, and if the Open Cable Detect signal is active (indicating the A cable is connected and controller has power), the drive enables its Select Compare signal.

The Select Compare signal enables the receivers and transmitters to the controller and also enables the Unit Selected signal. The drive is now ready to respond to further commands from the controller.

DUAL CHANNEL UNIT SELECTION

General

Dual channel drives are connected to, and can be selected by, either of two controllers. However, because the drive is capable of responding to only one controller at a time, the controllers must resolve contention for use of the drive. For this reason, there are functions associated with dual channel selection that are not necessary when selecting single channel units.

The logic on the dual channel steering card (location A07 on the logic chassis) is used to perform the following functions:

- Select - Logically connects the drive to the controller, thus enabling it to respond to commands from the selecting controller.
- Reserve - Reserves the drive so it can be selected at any time by the reserving controller, but prevents it from being selected by the other controller.
- Release - Releases drive from reserved condition.

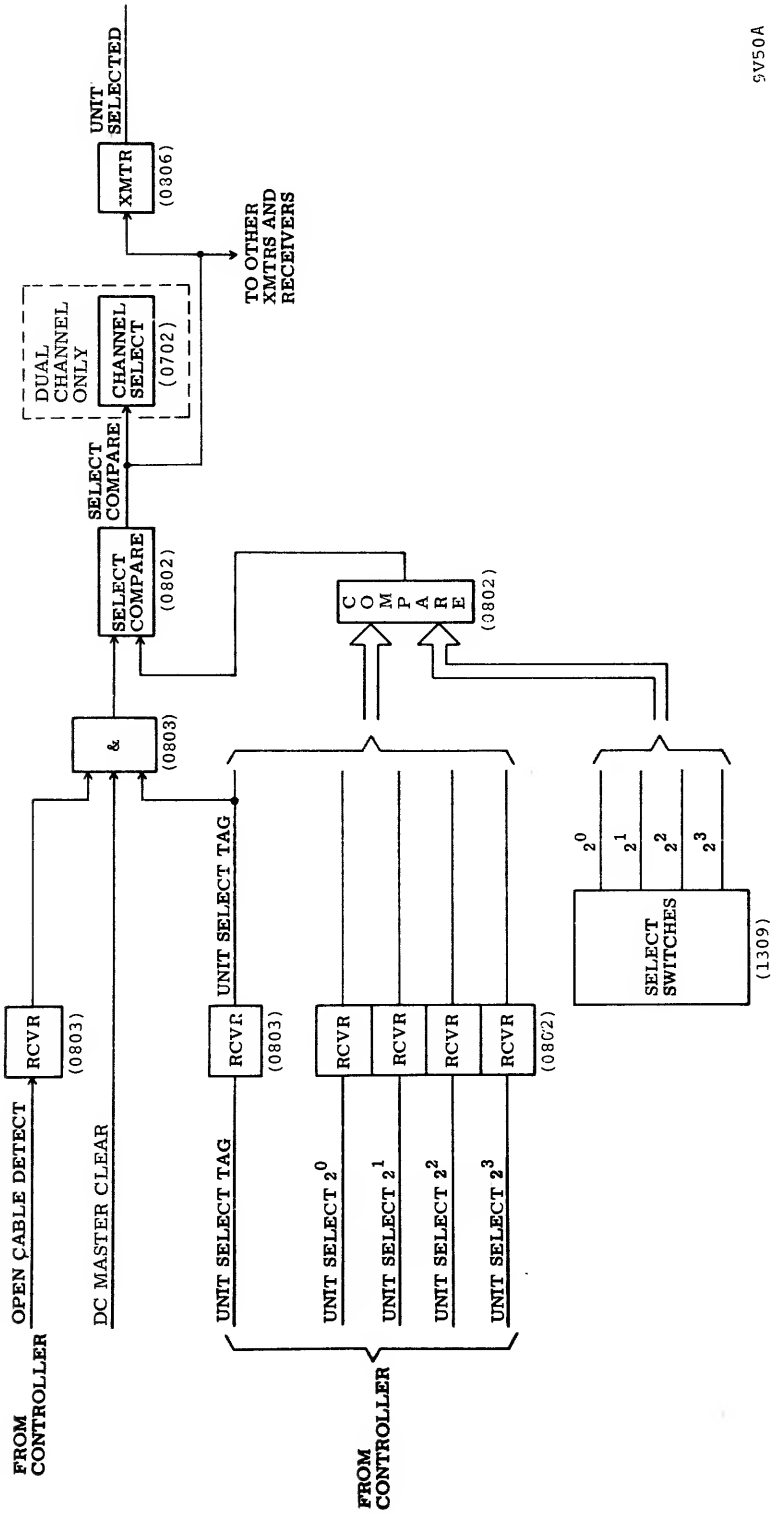


Figure 3-7. Unit Selection Logic (Single Channel)

- Priority Select - Allows the controller to force selection of the drive to the executing interface. Causes the other interface to deselect and release the drive.

- Disable - Allows disabling either channel interface during maintenance.

The following discussions describe each of these functions. It should be noted that because these functions are basically the same regardless of which channel is involved, they are described only as they relate to Channel I. Figure 3-8 shows the select logic associated with Channel I selection and table 3-2 describes the major elements on this figure. Figure 3-9 is a flowchart of the dual channel unit select and reserve functions.

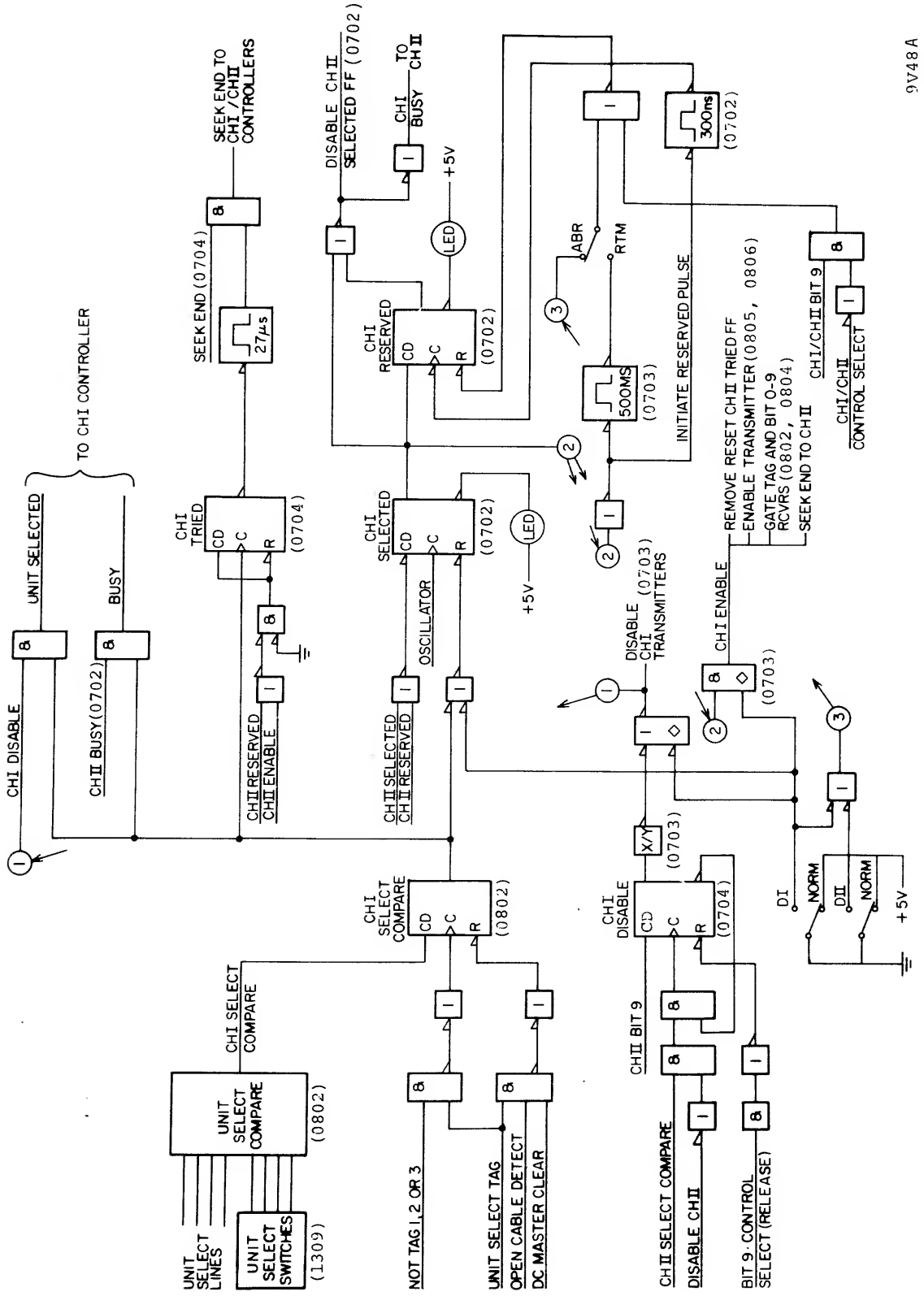


Figure 3-8. Channel I Dual Channel Select Logic

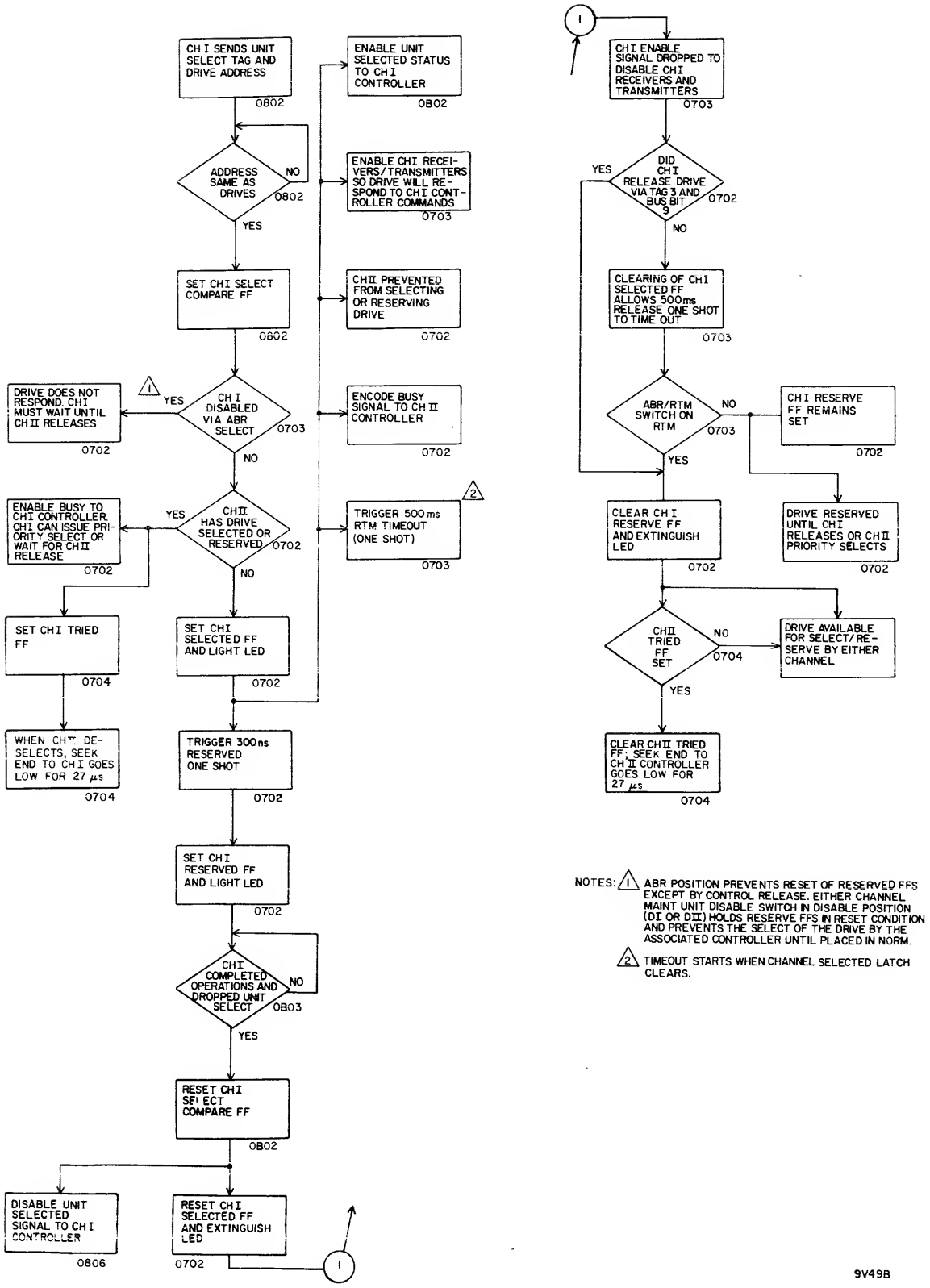


Figure 3-9. Dual Channel Select and Reserve Flowchart

TABLE 3-2. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS

Element*	Function
Release Timer Select	Determines whether the drive will be in ABR (absolute reserve) or RTM (reserve timeout) mode. If switch is in RTM position, drive is released from reserved condition after 500 milliseconds (nominal) of no channel activity. If switch is in ABR position, drive remains reserved until it receives a Release, Disable, or Priority Select command.
Release Timeout One Shot	Releases the drive by clearing the Reserve latch. The one shot is triggered when the drive is selected, and times out 500 milliseconds after the last command is received.
Channel I Disable latch	Sets if drive receives a Release or Priority Select command. This causes drive to be selected and reserved for controller issuing command and disables channel to other controller.
Channel I Disable Switch	Disables Channel I whenever it is set to DI (disable) position. It must be in NORM position during normal operations.
Channel I Reserved latch	Prevents other controller from selecting and reserving drive.
Channel I** Selected latch	Sets during select and reserve sequence and enables transmitters and receivers to Channel I controller.

Table Continued on Next Page

TABLE 3-2. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS (Contd)

Element*	Function
Channel I Select and Compare Logic	Compares logical address of drive with that sent by controller (see Single Channel Unit Selection).
Initiate Reserved Pulse	Generates 300-ns pulse whenever Select Compare signal goes active. Trailing edge of this pulse clocks Channel I and Channel II Reserve latches.
Channel I Select Tried latch	Sets if Channel I tries to select and reserve drive while it is already selected and/or reserved by Channel II. When drive is deselected and released by Channel II, or if it is manually disabled, this latch clears and activates the Drive Available Interrupt.
Drive Available Interrupt One Shot	Generates 27 microsecond pulse whenever either Tried latch clears. This pulse is sent to controller (associated with the Channel Tried latch that triggered the one shot) via the Seek End line.

* Includes only those elements directly concerning Channel I and shown in figure 3-8.

** The Channel Selected latches are alternately clocked by a free-running oscillator to prevent simultaneous selection.

Select and Reserve Function

The drive is both selected and reserved during the same sequence and this sequence is initiated by a Unit Select Tag accompanied by a logical address. However, the drive can be successfully selected and reserved only if none of the following conditions exists:

- Drive is already selected and reserved by other controller.
- Drive is not selected but is reserved by other controller.
- Channel attempting selection has been disabled by either a priority or maintenance disable function.

The following paragraphs describe how the drive is initially selected and also how it responds to a Unit Select Tag when it is selected, reserved, or disabled.

Assuming the drive is available (not selected, reserved, or disabled) and it receives a Unit Select Tag and logical address from the controller on Channel I, it compares the address received with that indicated by its logical address switches. If the two addresses are the same, the drive enables the Channel I Select Compare signal. The logic used to generate this signal is identical to that used in the single channel units.

The Select Compare signal causes the Channel I Selected and Reserved latches to set, enabling the receivers and transmitters to the Channel I controller. This signal also enables the Channel I Unit Selected signal that informs the controller that the drive is ready to accept further commands.

The drive remains selected to Channel I until the controller on Channel I drops its Unit Select Tag. At this time, the drive's Channel I Selected latch clears, disabling the drive transmitters and receivers for that channel. This also disables the Unit Selected signal thus informing the controller that the drive will no longer respond to commands. However, the drive remains reserved to Channel I (allowing Channel I to reselect while preventing Channel II from selecting) until the Channel I Reserve latch is also clear. This is cleared by either a release or priority select function.

If Channel I attempts to select and reserve the drive while it is selected and reserved by Channel II, the Channel I Select Compare signal is still generated as during the initial select and reserve sequence. However, the Channel I Select and Reserve latches do not set and, therefore, the attempt is unsuccessful. The drive still sends the Channel I Unit Selected

signal to the controller, but in this case, it is accompanied by the Channel I Busy signal. The Busy signal indicates that the drive is being used by Channel II.

The drive also sets its Channel I Tried latch, recording the unsuccessful attempt. When the drive is no longer selected or reserved by Channel II, this latch clears, causing Seek End to the Channel I controller to go inactive for 27 microseconds. This informs the controller that the drive is no longer selected or reserved.

If the Channel I controller tries to select the drive while Channel I is disabled (either by a priority or Disable function), the attempt is unsuccessful and no response is sent back to the Channel I controller.

Release Function

A channel reserve function can be cleared by one of the following operations:

- Executing a Release command
- No channel activity, provided the Release Timer Select switch is set to the RTM position
- Executing a Priority Select command on the other channel.

Priority Select Command

A Priority Select command deselects and/or releases the channel to the controller presently selected, and selects/reserves the drive to the controller issuing the priority.

Following a Priority Select command, the inactive channel is disabled until the channel issuing the command transmits a Release command.

Maintenance Disable Function

It is also possible to disable either channel by setting the Maintenance Unit Disable switch for that channel to the DI or DII position.

SERVO SYSTEM

The servo system contains the clocking and decoding logic required for seeking, track following, beginning of data detection (Index), and sector detection.

SERVO SURFACE

The HDA servo surface contains information that is prerecorded at the time of manufacture. The servo head reads this information from the servo surface; it is used by the servo circuitry to derive all of the signals used by the system. The servo head reads continuously as long as the drive is powered up and the disks are at operating speed.

Servo information on the servo surface is divided into four major bands as follows:

1. Outer guardband 2
2. Outer guardband 1
3. Normal servo band
4. Inner guardband

Head/Band Relationship

Figure 3-10 shows the relationship between the bands of information on the data and servo surfaces and the physical positions of the read/write and servo heads. (A band is a series of adjacent tracks that contain similar or related information.)

Each data surface has two data bands, one for each of the heads covering that surface. These data bands and their associated heads are aligned so that when the servo head is over the servo band on the servo surface, the data heads are also over the data bands on their respective surfaces. If the servo head moves out of the normal servo band and into a guardband, the data heads move out of their data bands.

The data and servo heads are also over the same relative points in their respective bands. For example, if the servo head is over track 10 in the servo band, all data heads are also over track 10.

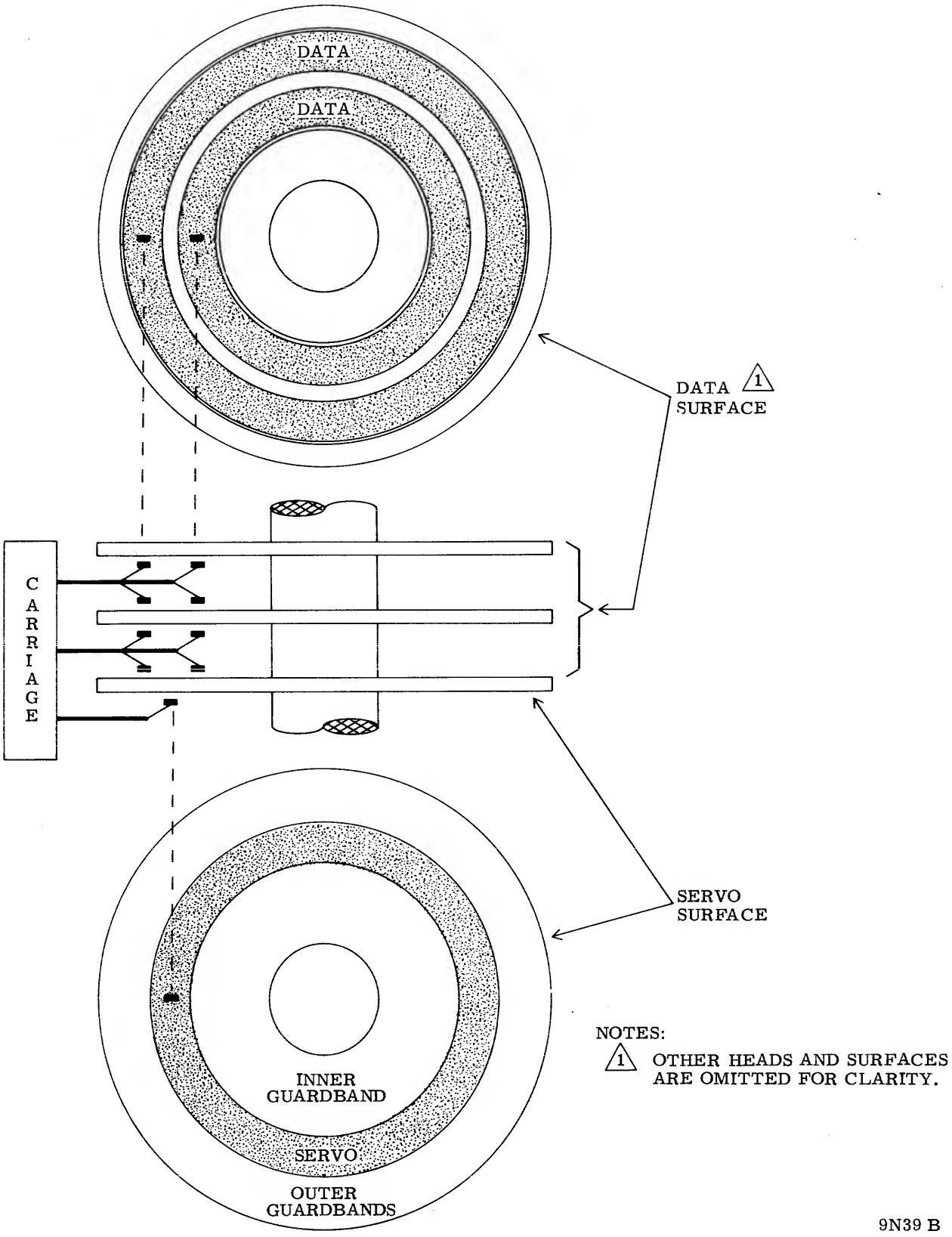


Figure 3-10. Servo to Data Surface Correlation

The fact that all heads are over the same relative points on their respective surfaces creates an imaginary cylinder. This imaginary cylinder permits the user to define seek distances in terms of cylinders (000 to 842). The fixed-head storage is also defined in terms of cylinders even though the cylinder concept just described does not apply.

Servo Tracks and Bytes

The servo information is recorded around the servo surface in 1089 concentric tracks and the information in these tracks is divided into 5 040 units called servo bytes. There are two types of tracks on the servo surface, odd and even. They are classified according to the type of servo byte they contain: odd tracks contain only odd bytes and even tracks contain only even bytes. Both types of bytes are shown on figure 3-11.

Figure 3-11 shows that a servo byte, regardless of type, contains four pulses: one index (not to be confused with index mark), one sync, and two quadbits. This figure also shows that if the byte is divided into six intervals, the difference between the two types of bytes is in the relative position of their quadbit pulses. In the odd servo byte, the quadbit pulses occur during the third and fifth (odd) intervals. In the even servo byte, the quadbit pulses occur during the fourth and sixth (even) intervals.

If the disks are rotating at their nominal speed of 3600 revolutions per minute, the servo byte frequency is about 300 kilohertz.

The odd and even tracks are recorded on the servo surface in an alternate manner (odd, even, odd, even and so on) with the outermost track being even and the innermost being odd.

Servo Patterns

In addition to being classified as odd or even, each servo byte is defined according to whether its index pulse is present or missing. A byte with the index pulse present is called a "zero" byte; one with its index pulse missing is calles a "one" byte. Normally, all servo bytes are zeros. A five byte pattern of both zeros and ones is inserted into the pattern of all zeros to orient the servo head. The specific pattern (of 1s and 0s) depends upon which area of the disk is to be identified.

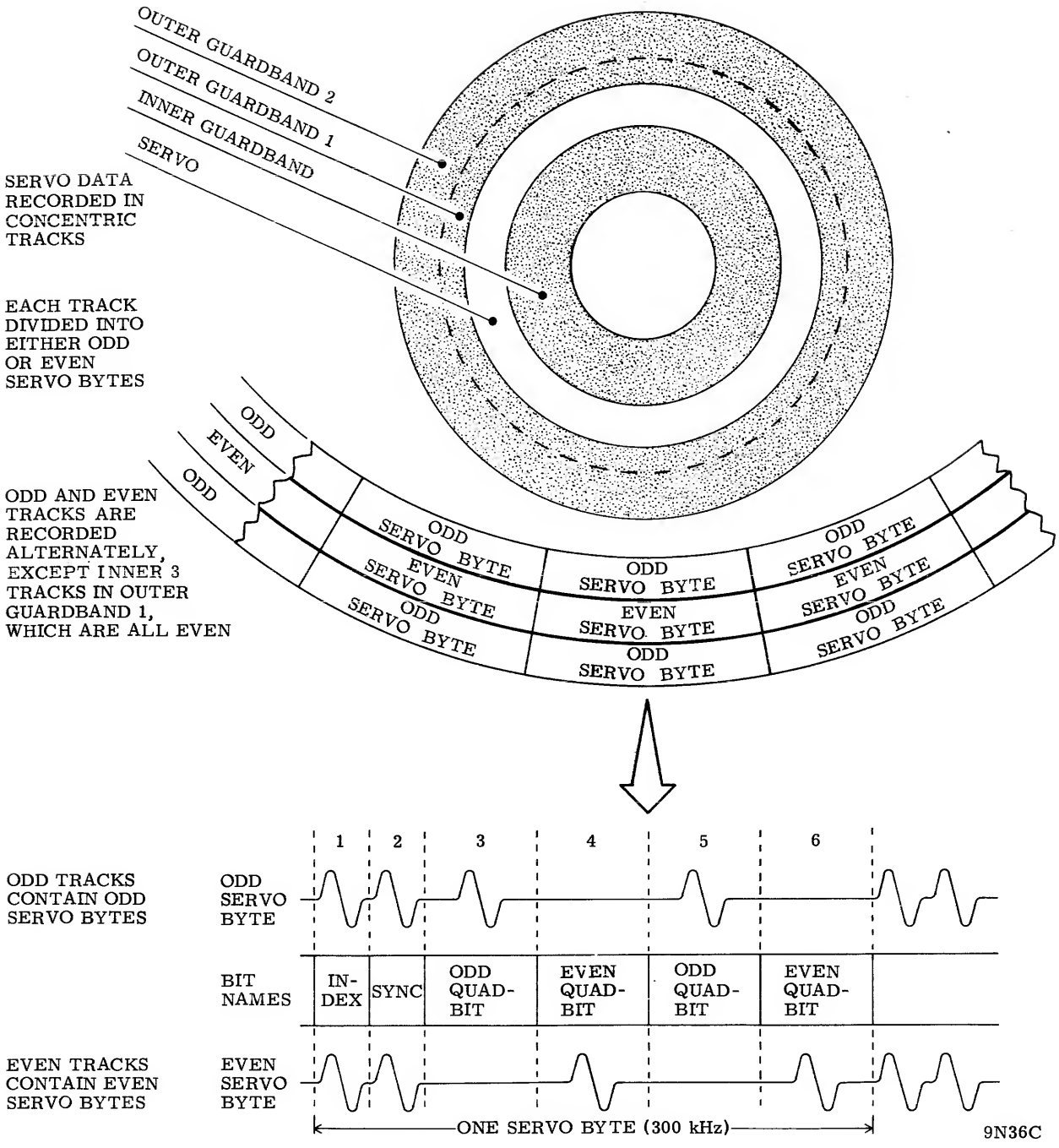


Figure 3-11. Servo Tracks and Bytes

The logic circuits recognize four of these servo patterns:

Area	Pattern
Outer Guardband 2	01110
Outer Guardband 1	01010
Inner Guardband	10011
Index Mark	01011 (in all tracks)

Figure 3-12 shows that the patterns identifying the guardbands are interspersed with 67 bytes of zeros; this 67-5-67... grouping repeats itself all the way around the guardband tracks. The index mark pattern occurs once in every servo track, and is always at the same angular position on the disk.

Figure 3-13 shows the servo patterns.

Servo Bands

Outer Guardband 2

This guardband is located nearest the outer edge of the disk. It is the area to which the heads retract when the disk stops spinning, and is therefore often referred to as the carriage home position. Its servo pattern is 01110.

Outer Guardband 1

Located between outer guardband 2 and the normal servo band, this guardband has a servo pattern of 01010. The three tracks on its inner periphery contain only even servo bytes; these tell the servo head when it has left the normal servoband area and is entering the outer guardband area.

Normal Servo Band

The normal servo band lies between the outer and inner guardbands. The junctions between even and odd servo tracks become significant in the normal servo band because it is over these junctions, known as physical cylinders, that the servo head is positioned during Seek operations. When the servo head settles over one of these junctions, the condition is called On Track. Except for the Index Mark, this band is filled with zero bytes.

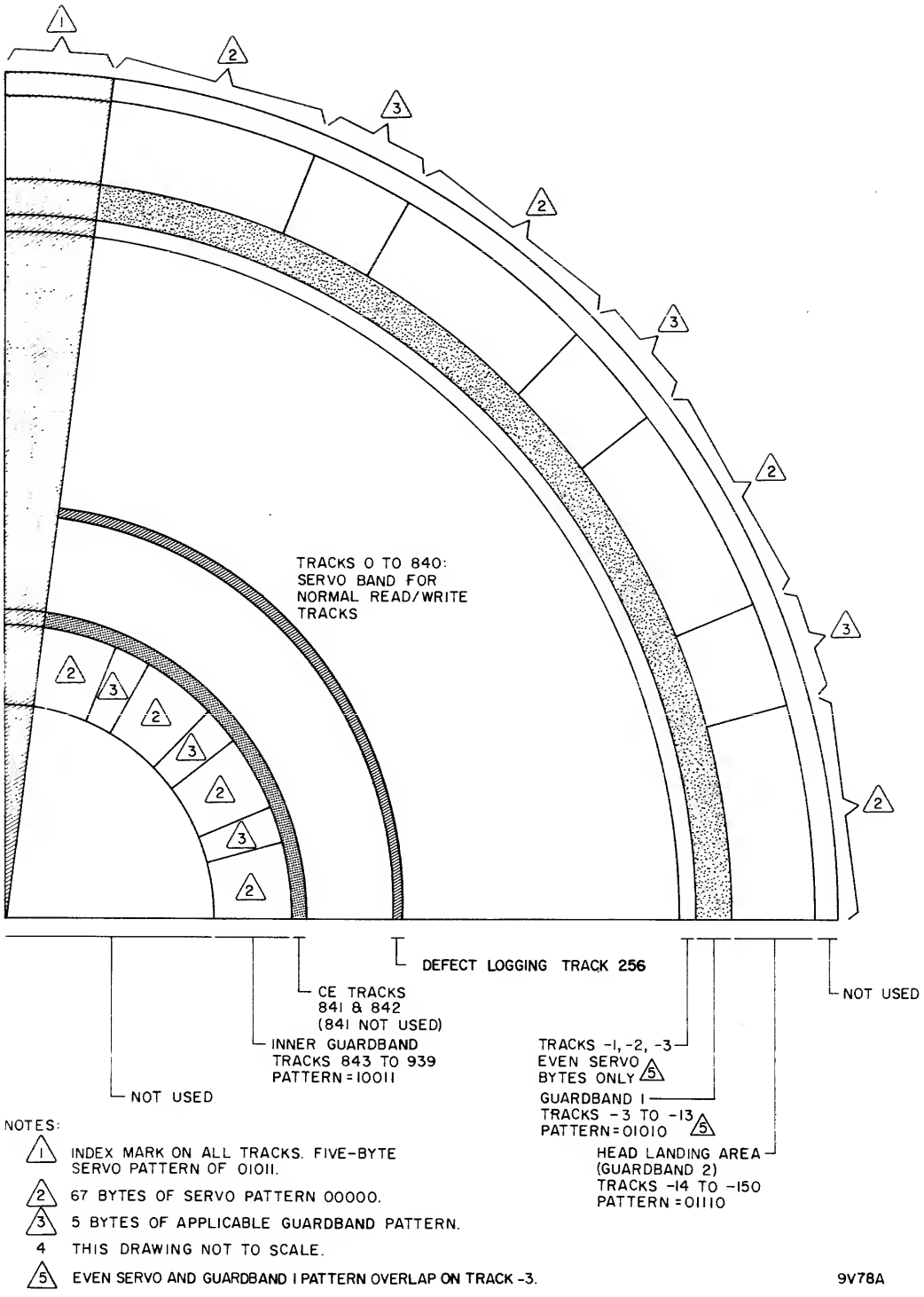
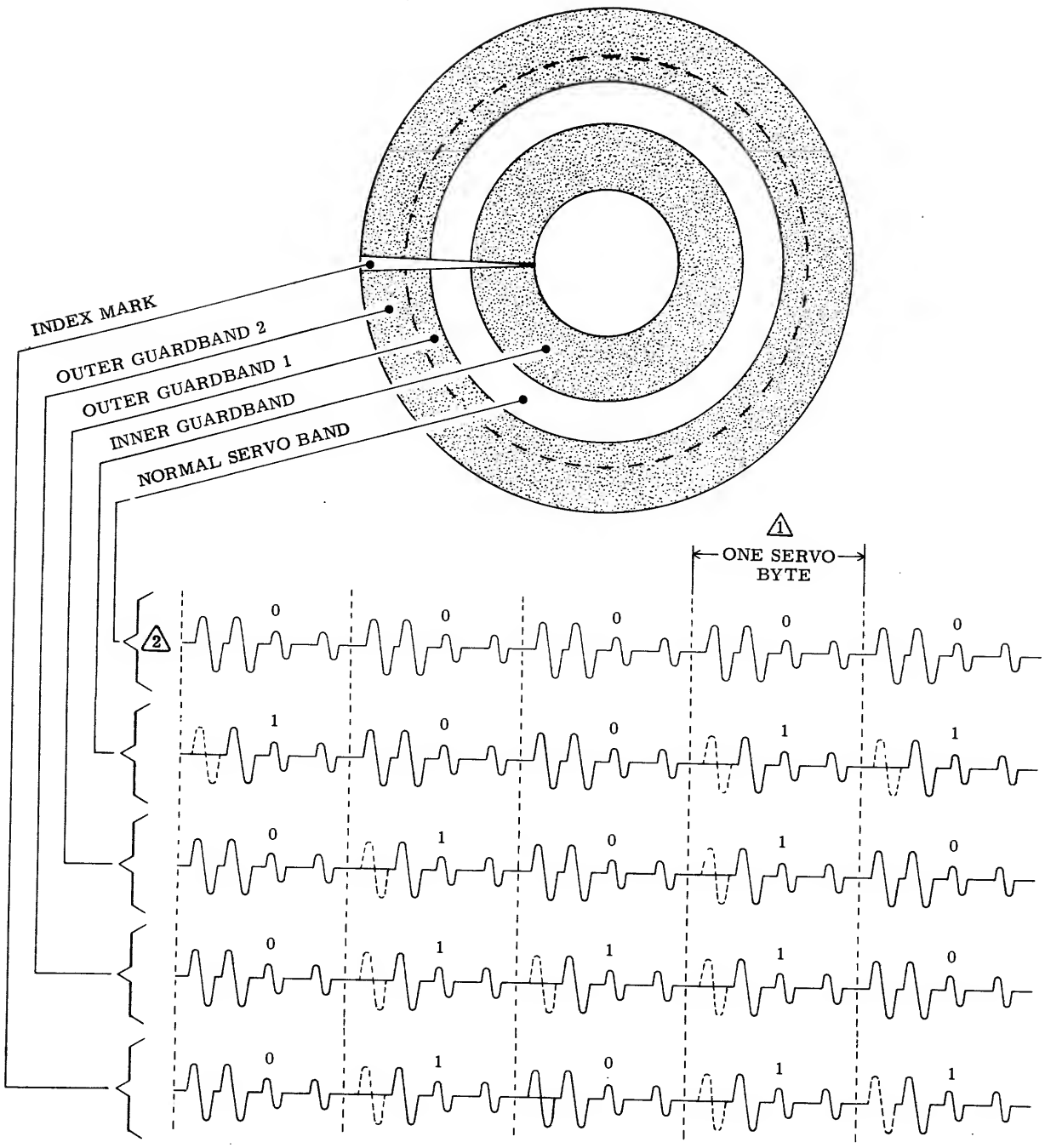


Figure 3-12. Servo Bands, Byte Layout



NOTES:

1. ONLY ODD SERVO BYTES (TWO QUADBITS) ARE SHOWN. NORMAL COMPOSITE PATTERN CONTAINS FOUR QUADBITS.
2. SHOWN FOR REFERENCE ONLY. NOT RECOGNIZED BY LOGIC CIRCUITS AS A SERVO PATTERN.

10B61

Figure 3-13. Servo Patterns

Inner Guardband

The servo tracks nearest the center of the disk form the inner guardband. The band is used to determine when the heads have moved out of the data area during a forward Seek. Its servo pattern is 10011.

SERVO LOGIC

The servo logic, shown in figure 3-14, controls the movement of the voice coil motor. It also generates several clocks used within the servo logic and by other logic in the unit. The servo logic consists of the following major components:

- Servo decode and machine clocks
- Velocity detection
- Position control.

Table 3-3 describes the major signals generated by the servo logic.

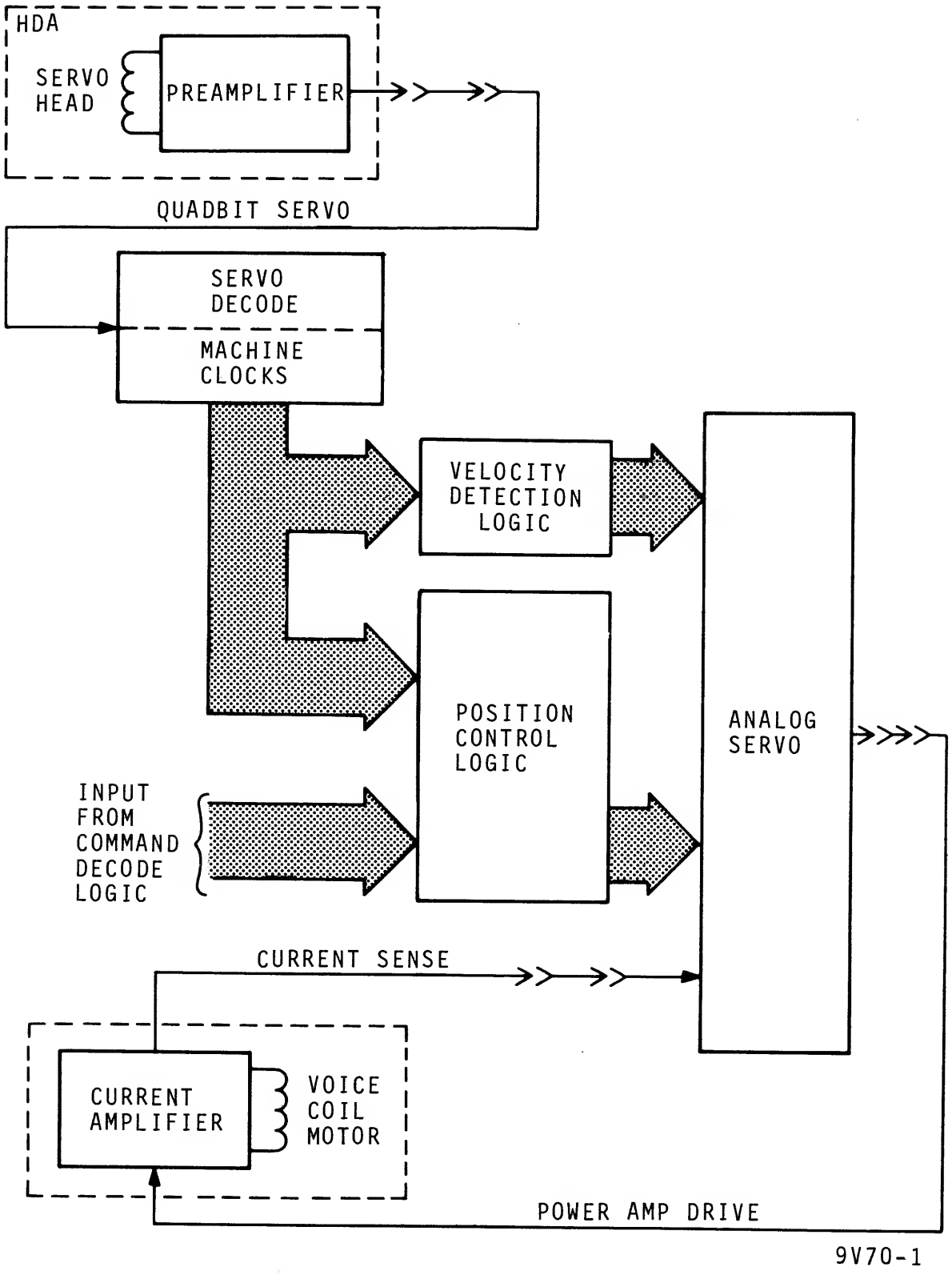


Figure 3-14. Servo Logic Overview

TABLE 3-3. SERVO LOGIC SIGNALS

Signal Name	Description
±Position (analog)	Defines the position of the servo head with respect to the servo tracks. The voltage amplitude of both signals is zero (servo null) when the servo head is equidistant between two servo tracks. The read/write heads are then centered over their data tracks. Both signals are maximum (but of opposite polarity) when the servo head is located over a servo track. The polarity of the signal is determined by the state of the Slope signal and the current position of the heads (odd or even servo track). The frequency of ±Position varies in direct relation to the speed of the voice coil motor.
+Slope	Orients the polarity of the ±Position signals with respect to the servo tracks. the +Slope signal is inactive (low) following the Power-On RTZ seek (even servo track). On subsequent seeks, the signal level changes only during odd seek lengths, that is, seeks where the heads move an odd number of cylinders to the new destination.
+Integrator Enable	Activates the Fill In Integrator logic when the seek operation has <128 tracks to go.

Table Continued on Next Page

TABLE 3-3. SERVO LOGIC SIGNALS (Contd)

Signal Name	Description
-Forward	Directs the servo head to move in the forward direction (toward the spindle).
-Reverse	Directs the servo head to move in the reverse direction (away from the spindle).
+Power Amp Drive (analog)	Controls the acceleration and direction of the voice coil motor. The acceleration is determined by the amplitude of the current on this line. If the current polarity is positive, the voice coil motor causes the servo head to move in the forward (toward the spindle) direction. Negative polarity causes a reverse movement.
+Coarse	Indicates that 4 V (positive or negative) has been detected for the second time on the Position signal with <1 track to go.
+Fine	Indicates that On Track has been detected during settle-in.
+Fill In (analog)	Supplements the current level of the +DAC input to the summing gates. This ensures that the +DAC (desired velocity) retains a smooth decline in amplitude as the servo head reaches On Cylinder. +Fill In is activated when the seek has <128 tracks to go.

Table Continued on Next Page

TABLE 3-3. SERVO LOGIC SIGNALS (Contd)

Signal Name	Description
±DAC (analog) ±Velocity (analog)	±DAC corresponds to desired velocity. ±Velocity corresponds to the actual velocity. These signals are combined to produce an error signal that moves the servo head to the desired destination in a minimum time without overshoot or oscillation.
+Linear Region	Defines when the ±Position signals are within ±2.4 V of zero.
+Current Sense (analog)	Produces a signal that is directly proportional to, and with the same polarity as, the current applied to the voice coil motor.
±Track Crossing Pulse	A 20-microsecond pulse that occurs each time ±Position voltage passes through zero.
-On Track	Indicates that ±Position signals are within 0.85 V of zero when the carriage is moving. The pulse width is determined by the frequency of the ±Position signals. Signal is active continuously when On Cylinder.
+Gated Servo Clock	A timing signal with a 300-kHz frequency used to synchronize the servo PLO to the data from the servo head. Synchronization occurs when the drive motor comes up to speed.

Table Continued on Next Page

TABLE 3-3. SERVO LOGIC SIGNALS (Contd)

Signal Name	Description
+PLO Clock	A timing signal with a 4.83-MHz frequency used for motor at speed detection, position decoding, and to generate the 1F (9.67 MHz) and 2F (19.34 MHz) clocks.
-Sector Count Pulse	A timing signal with a 300-kHz frequency used for guardband and index detection.
±1F Clock	A timing signal with a 9.67-MHz frequency used for sector decoding, PLO locked-to-data detection, read/write logic.
+2F Clock	A timing signal with a 19.34-MHz frequency used for write compensation.

Servo Decodes and Machine Clocks

The servo decode logic (figure 3-15) converts the analog signals produced by the preamplifier (quadbits) into digital information of the same frequency: Servo Data. This information is then used to generate the following timing signals:

- Gated Servo Clock
- 4.83 MHz Clock (PLO Clock)
- Sector Counter Pulse
- 9.67 MHz Clock
- 19.34 MHz Clock
- Index Gate

Each quadbit read from the HDA servo surface generates a Servo Data pulse. Each group of six Servo Data pulses generates a Gated Servo Clock (300 kHz frequency). The interval between each Gated Servo Clock constitutes a servo byte. One Sector Count pulse and one Index Gate pulse are generated for every servo byte. A total of 5 040 servo bytes are generated during one track revolution.

The servo PLO (phase-locked oscillator) generates the basic 4.83-MHz clock frequency. This frequency is divided by 16 to produce the Gated Servo Clock.

The write PLO is locked to the output frequency of the servo PLO. After synchronization, the output is quadrupled to produce the 19.34-MHz clock, and then divided to produce the 9.67-MHz clock.

Velocity Detection

The velocity detection circuit (figure 3-16) determines the speed of the carriage between tracks on the disk surface. The Velocity signal is derived from two sources. When the servo head is Located within the Linear region between two servo bands (see figure 3-17), the Velocity signal is obtained by differentiating the Position signal and integrating the Current sense signal. When the servo head is outside the Linear region, the Velocity signal is obtained by integrating the Current Sense signal. The circuitry uses the Reverse signal to ensure that the integrated current sense maintains the proper polarity regardless of seek direction.

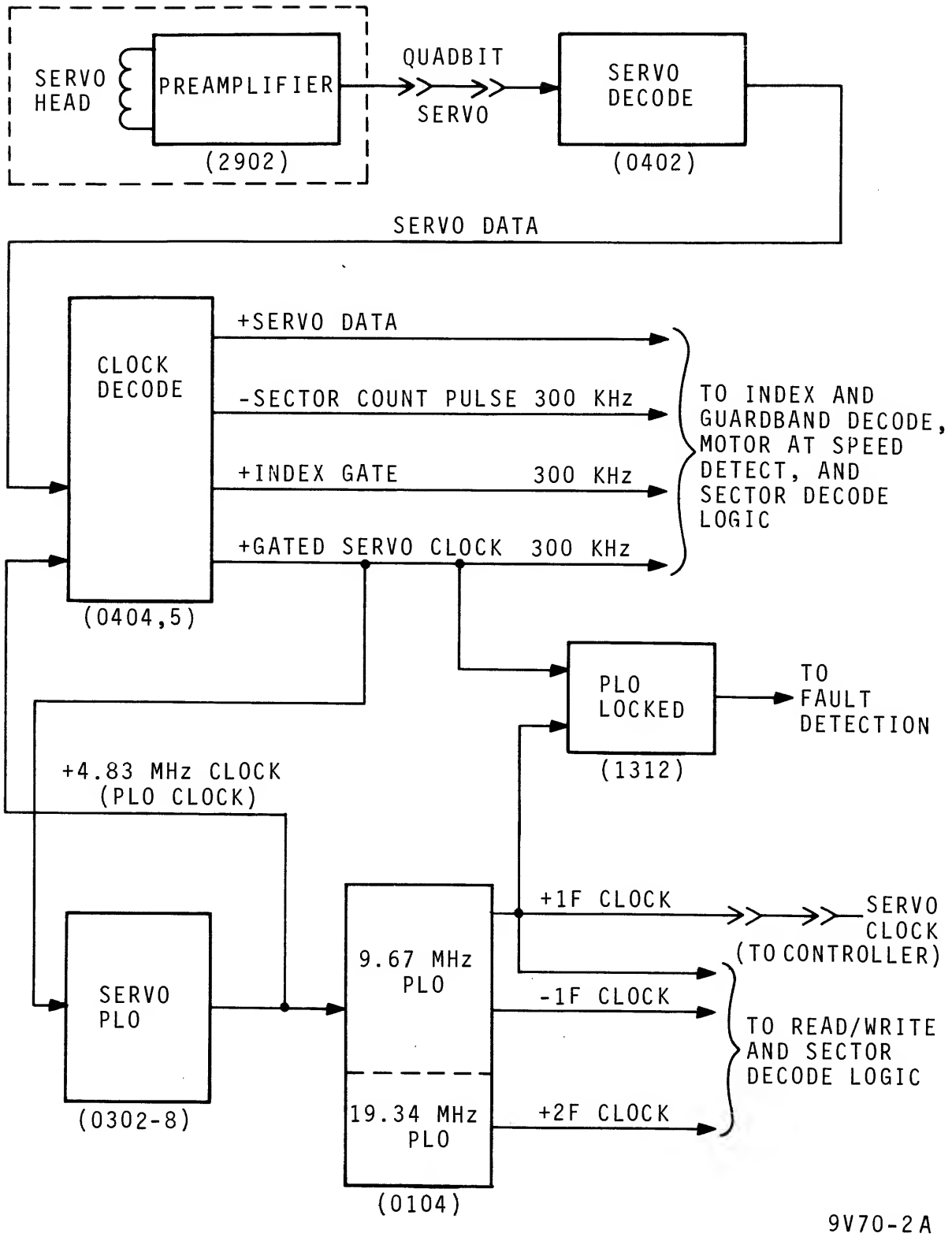


Figure 3-15. Servo Decode and Machine Clocks Logic

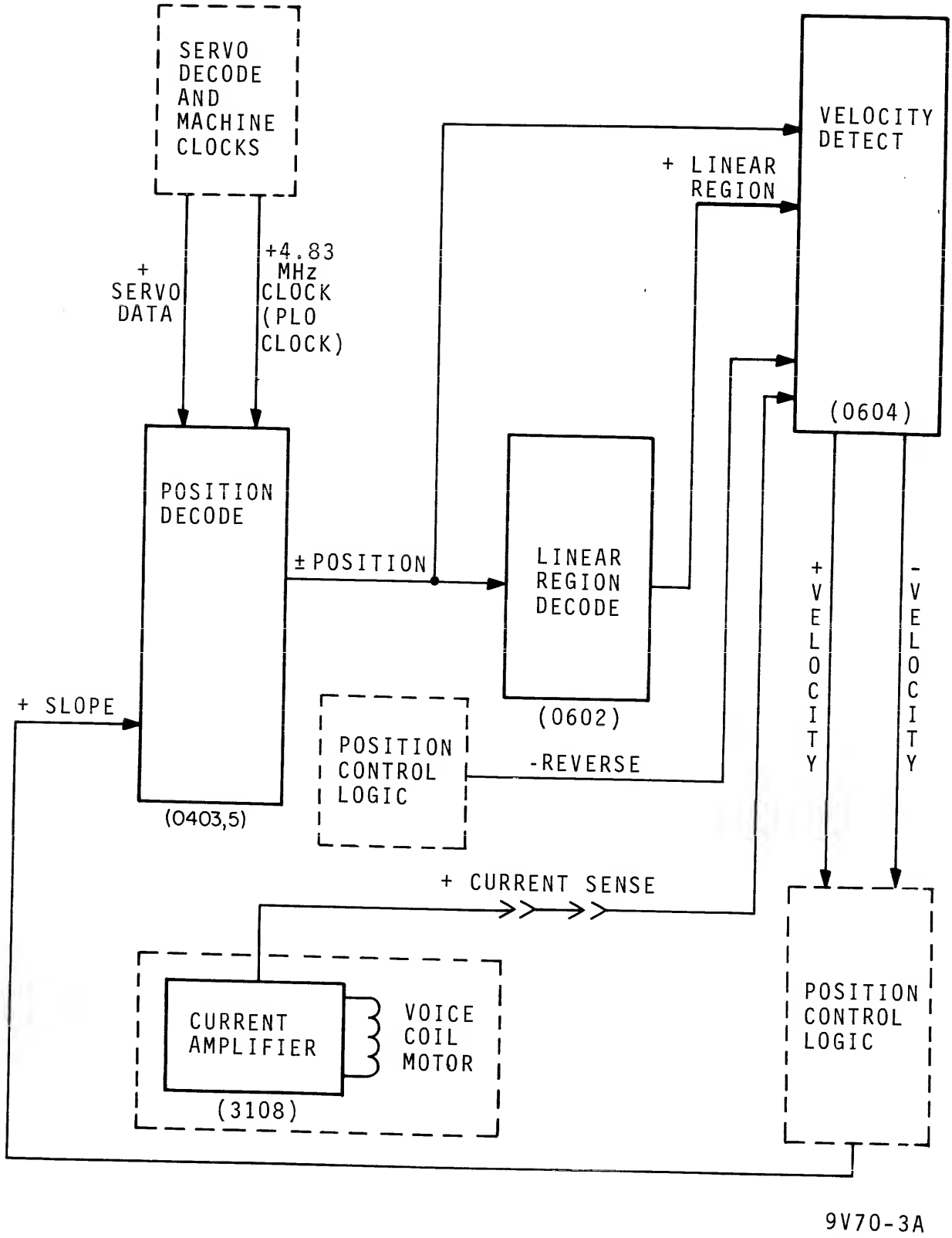


Figure 3-16. Velocity Detection Logic

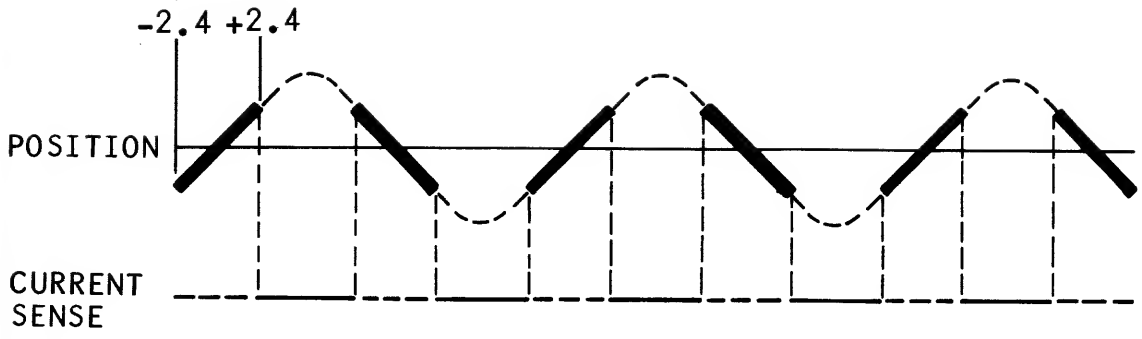


Figure 3-17. Linear Region Detection

Position Control

The position control logic (figure 3-18) compares the new cylinder address with the current address. It then calculates the distance, direction, and optimum speed to reach the new address. After initiating the move, the position control logic continuously adjusts the speed to avoid overrunning the new address.

At the beginning of a seek operation, the microprocessor in the position control logic formulates a difference count that denotes the distance and direction of the seek. The microprogram uses the difference count to reference a table of values in micro-memory that corresponds to the optimum velocity curve for a seek of that particular distance and direction. The microprocessor controls the seek by continuously changing the distance and desired velocity parameters, and compensating for differences between desired velocity and actual velocity. A separate fill-in integrator circuit smooths out changes in desired velocity caused by repeated changes to the velocity parameters. The fill-in integrator is activated when the seek operation has fewer than 128 tracks left to go.

The microprocessor activates Coarse when the seek has less than one track to go and the Comparator Position signal is detected. See figure 3-19. Activating Coarse disables the summing gates (Velocity and DAC signals) and enables settle-in logic. The settle-in logic generates an off track error signal by differentiating Position to obtain Velocity, and then subtracting Velocity from Position.

The microprocessor activates Fine after a 20-microsecond timeout following the last On Track signal at the target track. Activating Fine disables the settle-in logic and enables the track following logic. Track following drift is detected by checking for more than 0.85-V on the Position signal.

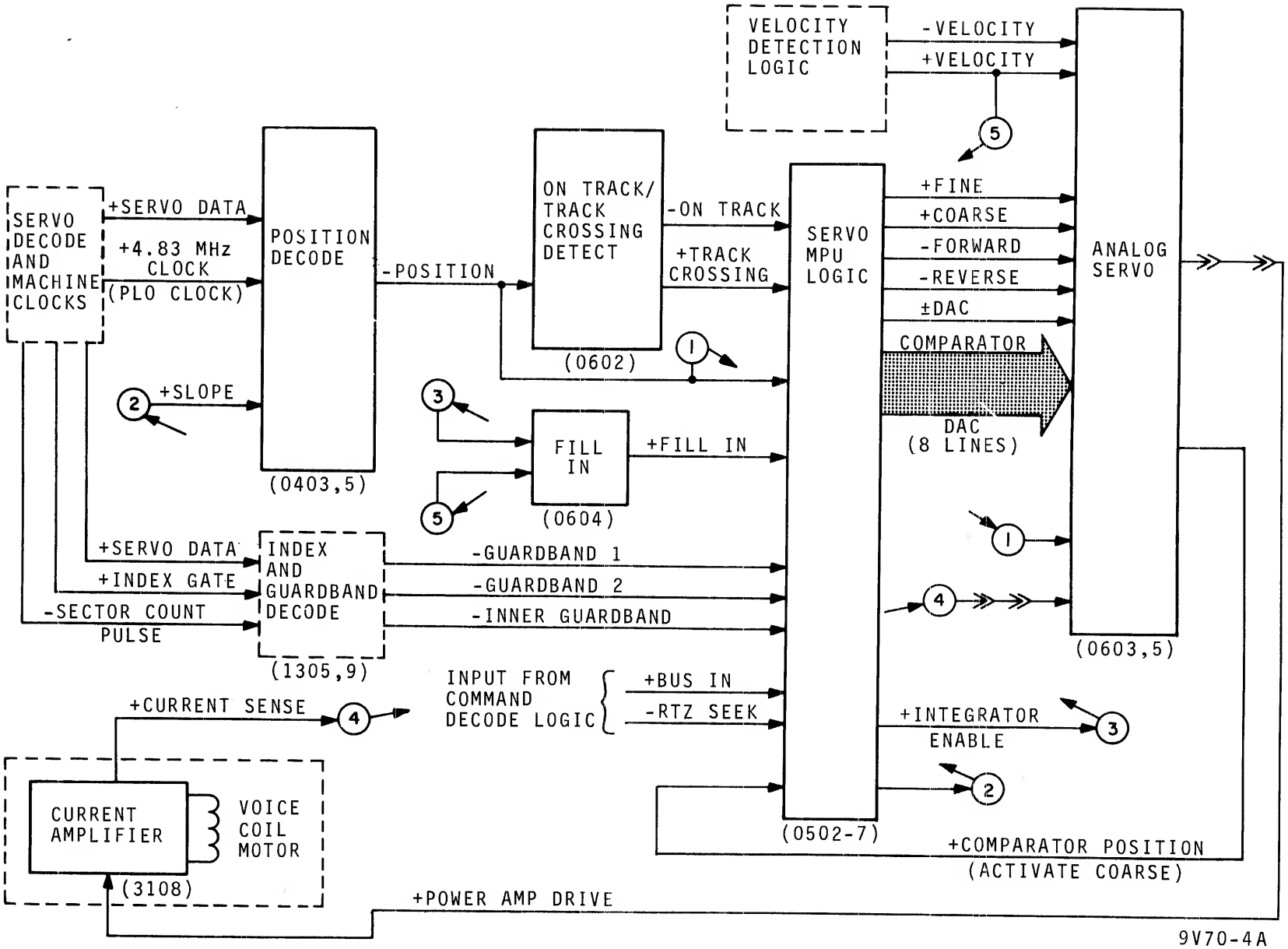


Figure 3-18. Position Control Logic

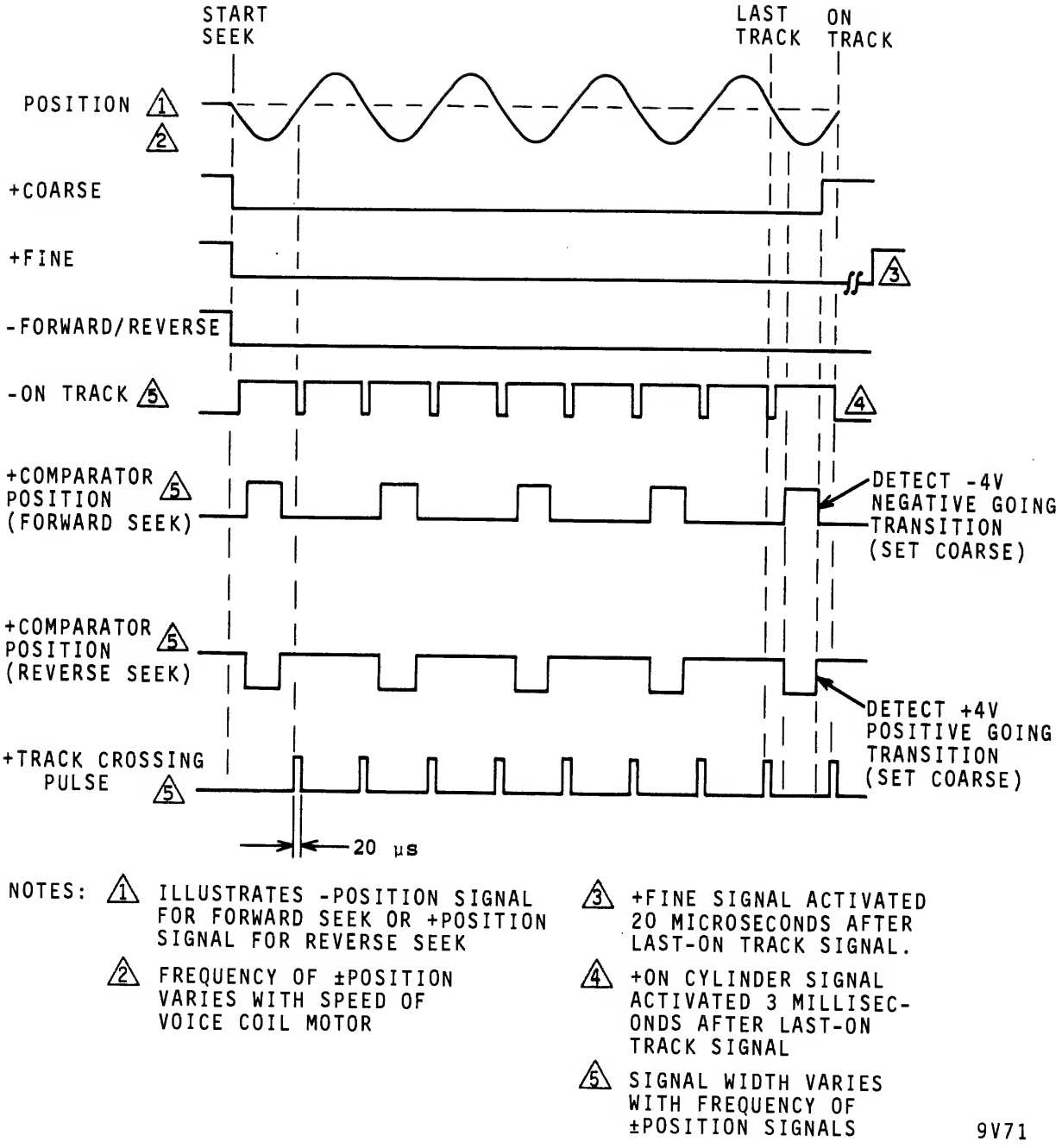


Figure 3-19. Servo System Timing

TYPES OF SEEKS

The servo microprogram performs two types of Seek operations, Normal Seek and Recalibrate (RTZ) Seek. The microprogram steps involved in each type of seek are described in figure 3-20.

Normal Seek

Normal seeks are initiated by controller command. The seek argument is decoded and used to move the heads from one location to another on the disk surface. A normal seek to a cylinder in the range from 896 to 898 (fixed head cylinders) does not cause servo activity and is treated as a zero-track seek by the servo microprocessor.

Recalibrate(RTZ) Seek

The RTZ seek moves the read/write heads from an unknown location on the disk surface to cylinder 000. An RTZ seek can be initiated either by the controller or by microprogram control.

GUARDBAND AND INDEX DETECTION

Detection of the index mark and guardband patterns is performed by the logic shown on figure 3-21. This figure also shows the patterns and basic timing.

Servo bytes with missing index bits are detected by the index bit detection circuit. The inputs to this circuit are the Servo Data and Index Gate signals.

The Servo Data signal is derived from the quadbit signals transmitted by the servo head. A missing quadbit results in a missing Servo Data signal.

The Index Gate signal is also derived (indirectly) from the Servo Data pulses read from the disk. This signal is active only during the time the index servo pulses should appear (regardless of whether or not they actually do).

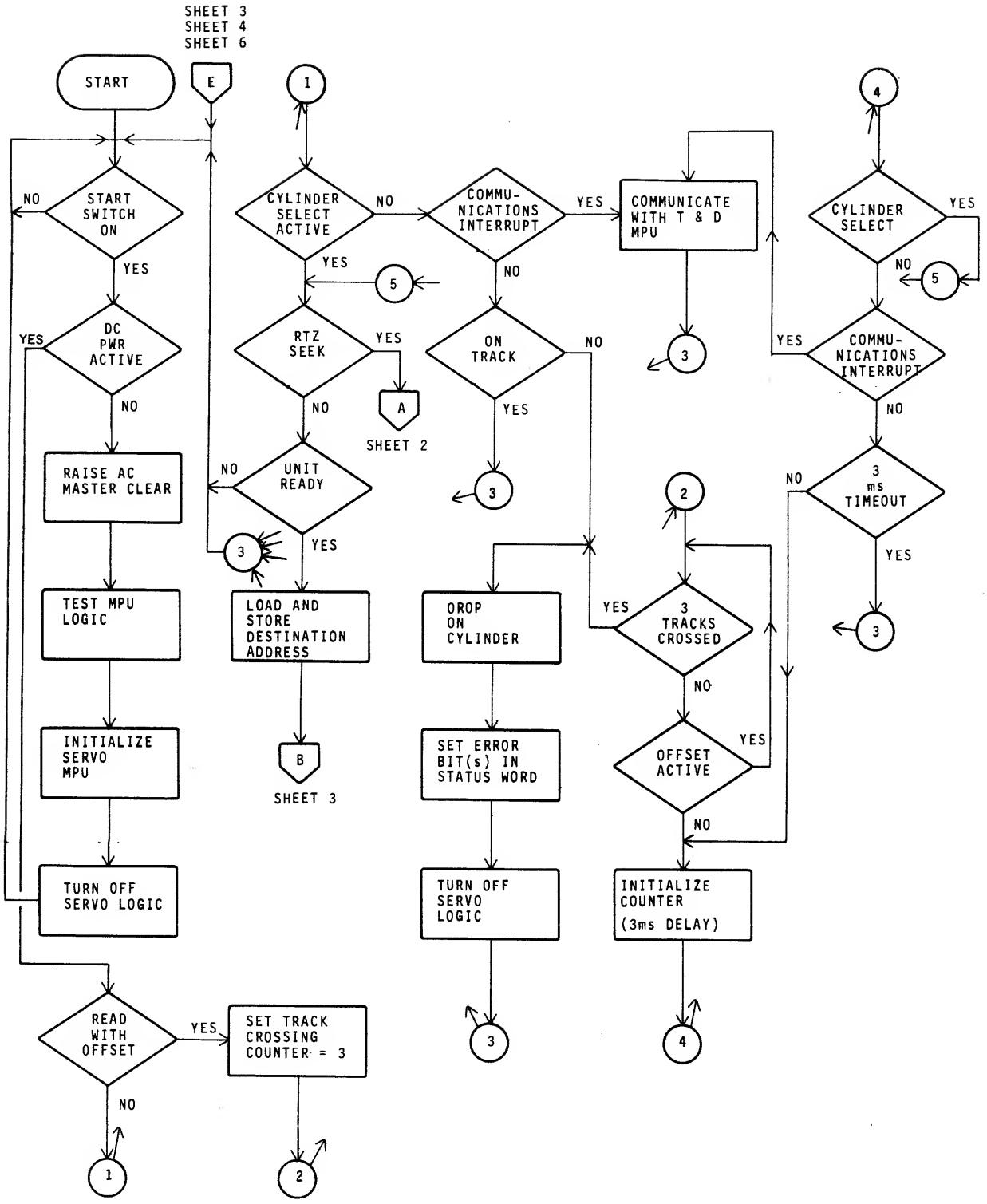


Figure 3-20. Servo Microprogram (Sheet 1 of 6)

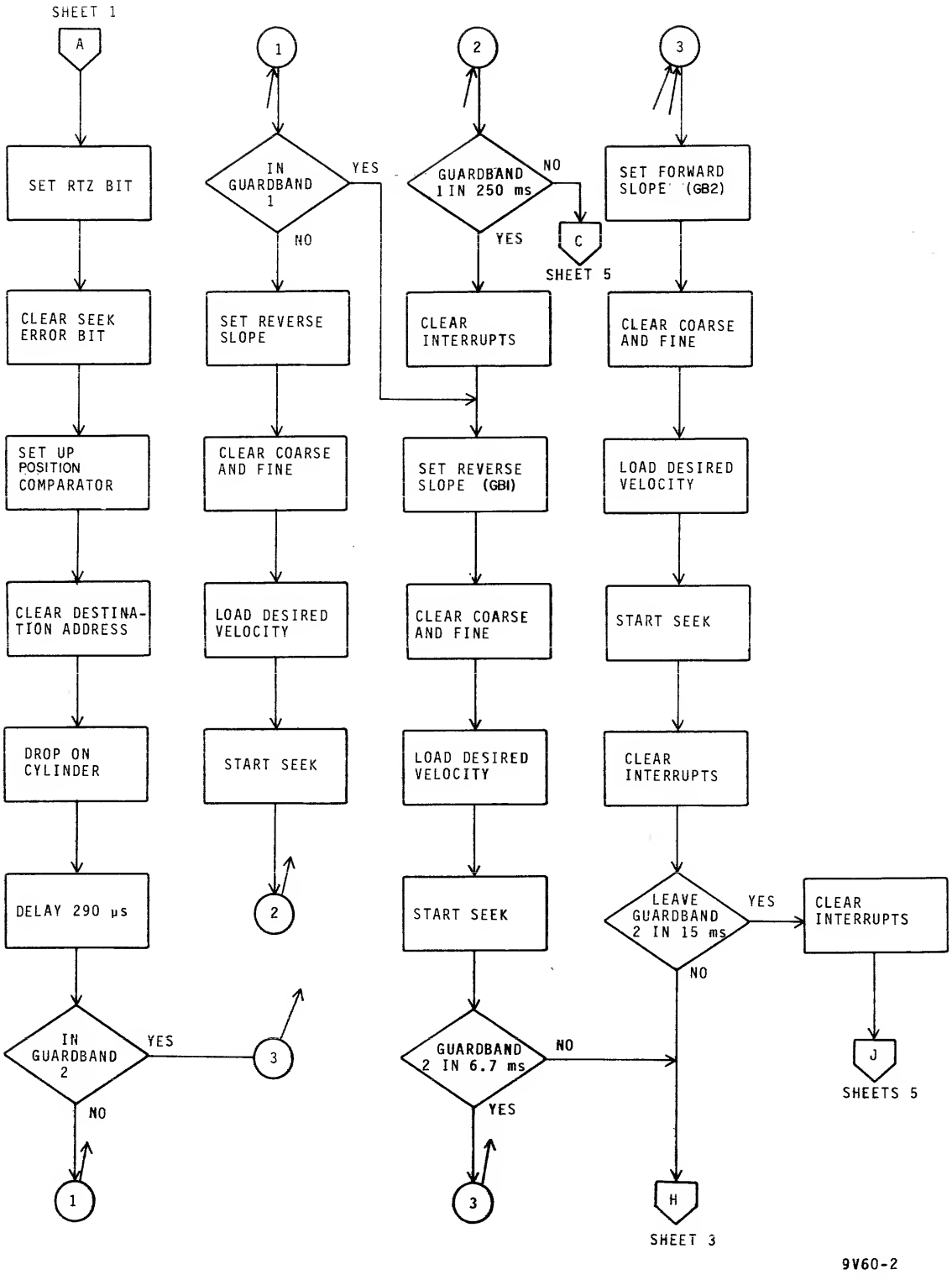


Figure 3-20. Servo Microprogram (Sheet 2)

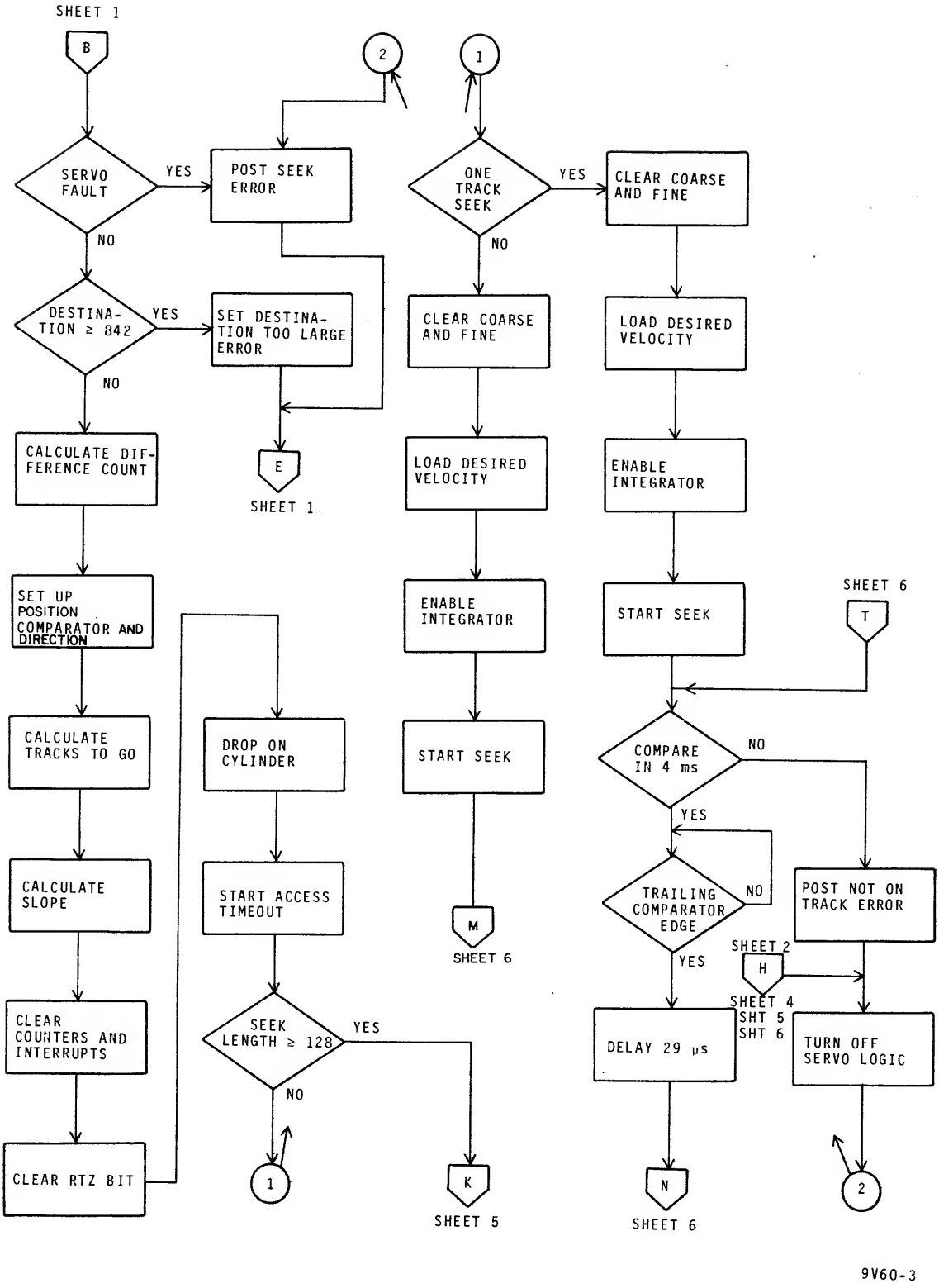


Figure 3-20. Servo Microprogram (Sheet 3)

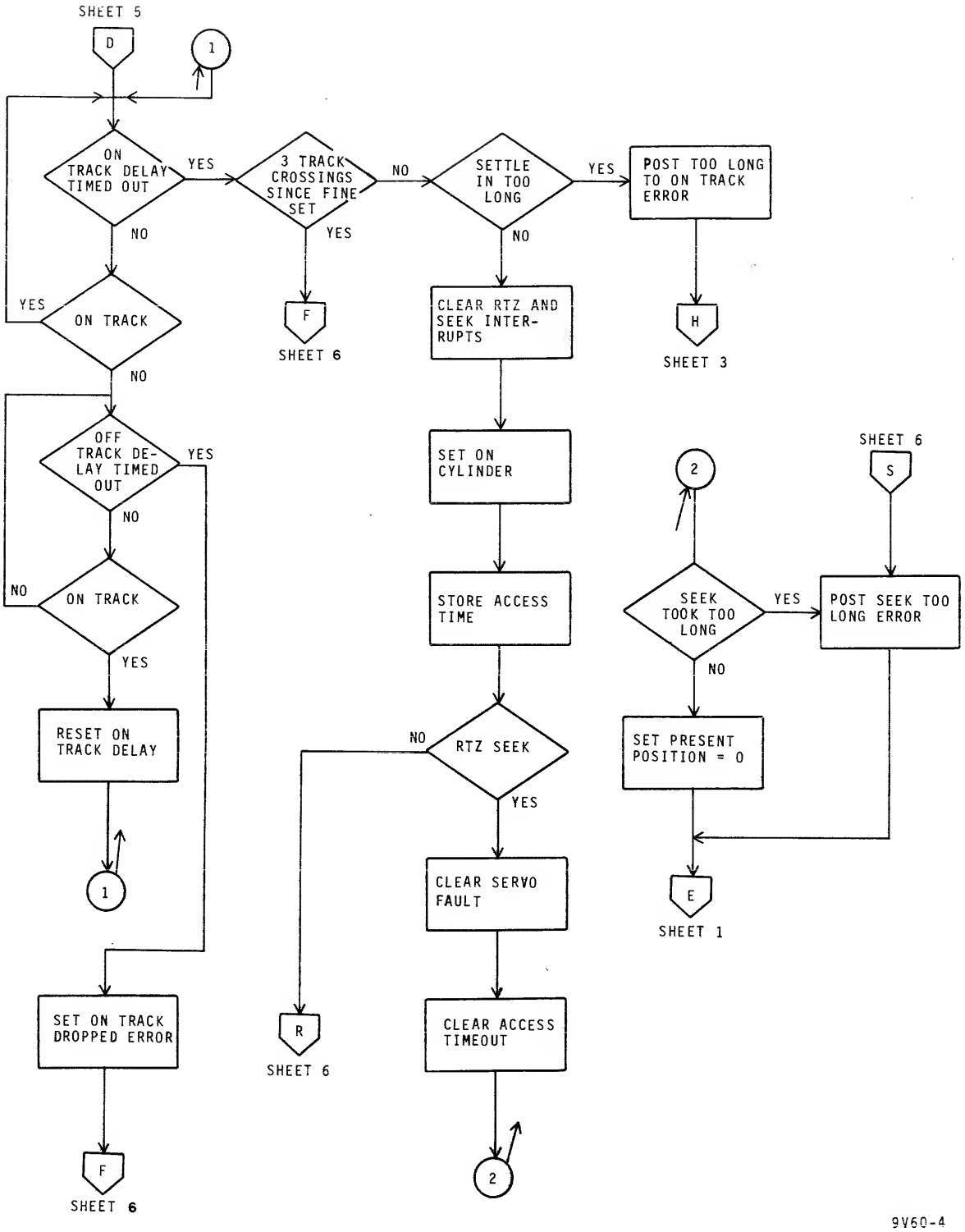


Figure 3-20. Servo Microprogram (Sheet 4)

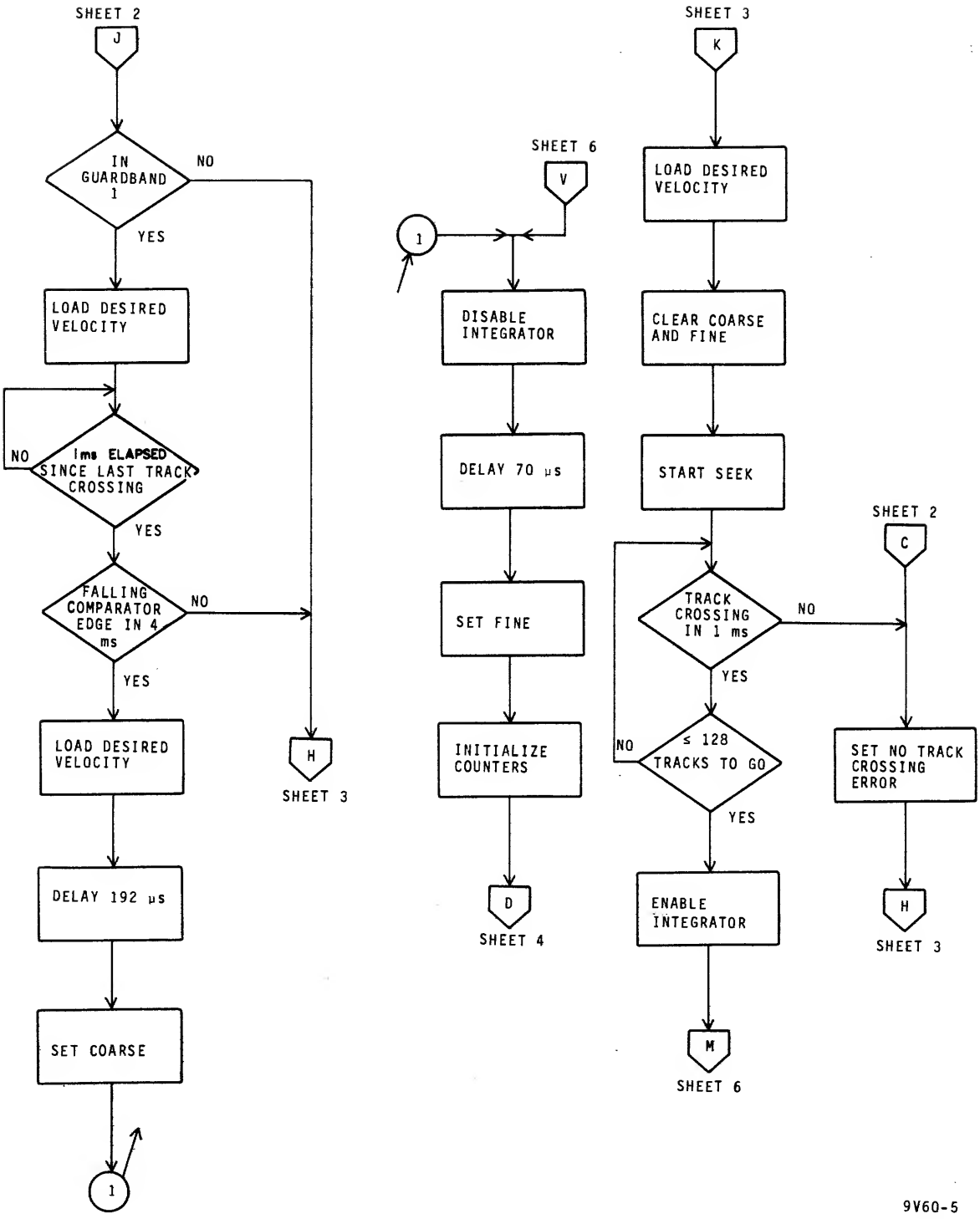


Figure 3-20. Servo Microprogram (Sheet 5)

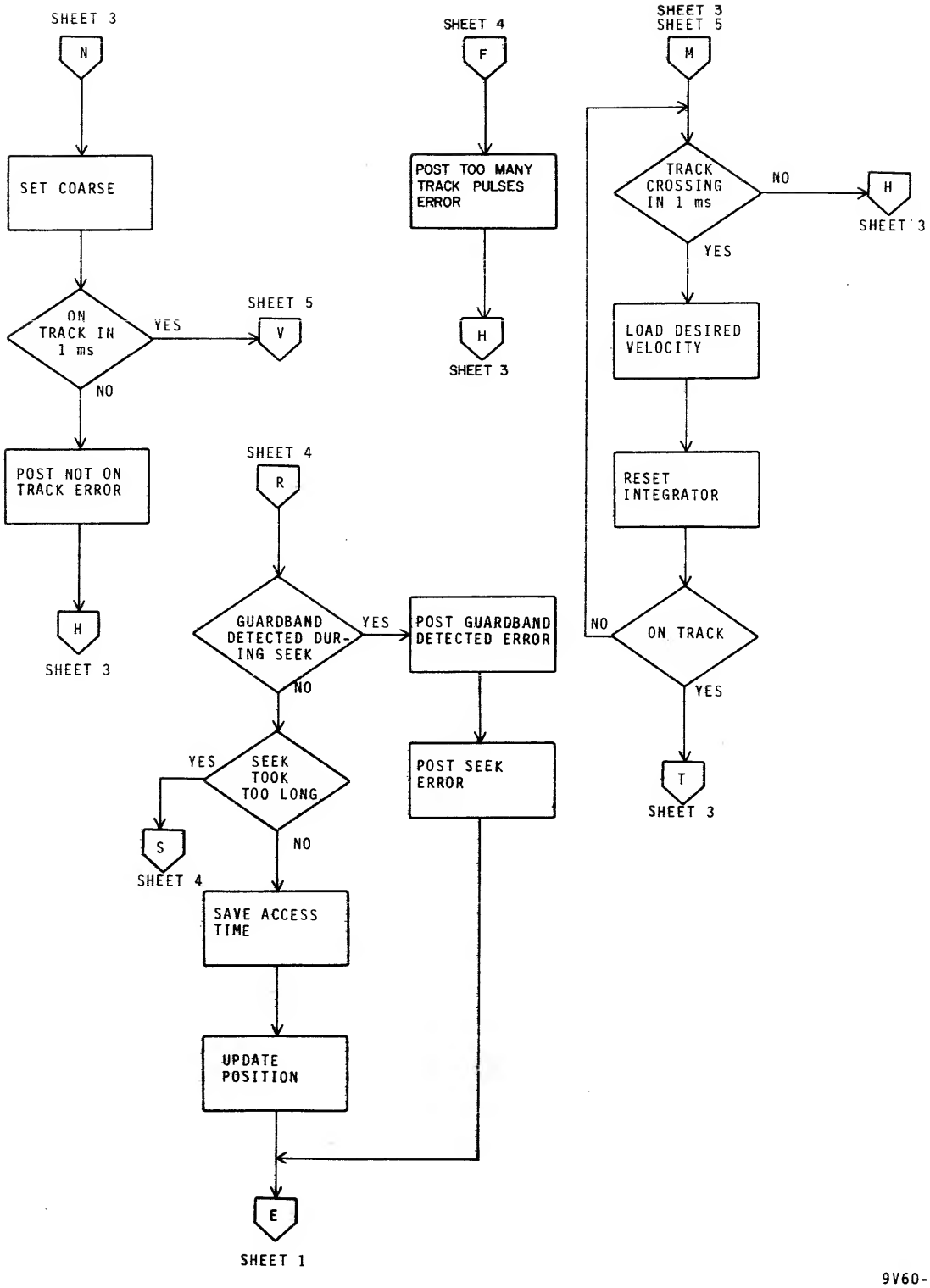
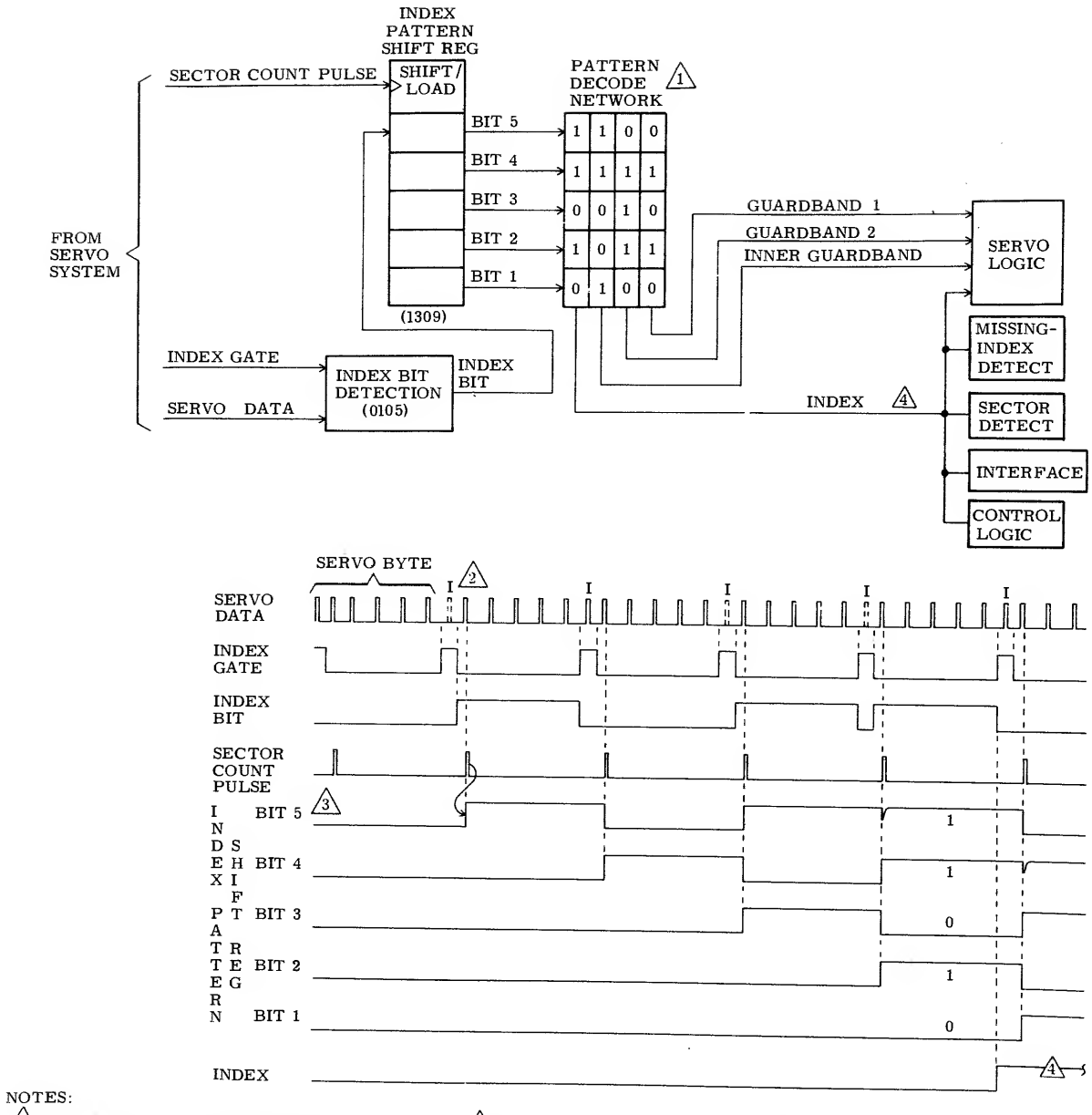


Figure 3-20. Servo Microprogram (Sheet 6)



NOTES:

1. SHOWS PATTERN NECESSARY FOR DECODING OF VARIOUS SIGNALS.
2. SERVO DATA PULSES CORRESPONDING TO INDEX SERVO PULSES ARE INDICATED BY "I". MISSING SERVO DATA PULSES INDICATED BY DASHED PULSES.
3. ONLY INDEX PATTERN IS SHOWN.
4. STAYS UP UNTIL INDEX PATTERN SHIFT REGISTER CONTAINS ALL ZEROES (5 SECTOR COUNTS).

9V72A

Figure 3-21. Guardband and Index Detection

By using both the Servo Data and Index Gate signals, the index bit detection circuit generates Index Bit each time the index bit of a servo byte is missing.

The Index Bit signal is the input to the first stage of the Index Pattern shift register. This register loads the Index Bit signal into its first stage (and also performs its shift) each time a Sector Count pulse occurs. These pulses occur once per servo byte.

When the Index Bit signal is a zero, (indicating the index servo pulse is present) a zero is loaded into the Index Pattern shift register. However, when this signal is active or high (indicating the index servo pulse was missing) a one loads into the register.

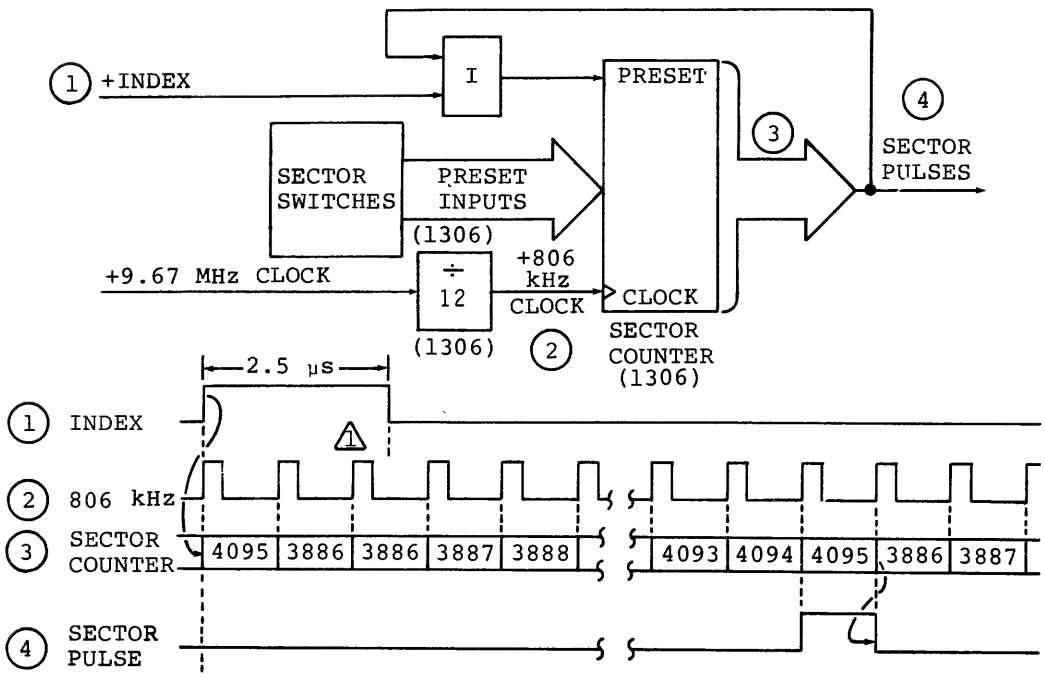
The contents of the shift register are continuously being examined by the pattern decoding network. Whenever either the Index Mark or a guardband pattern is detected, the appropriate decoder output goes active. These outputs are used as shown in figure 3-22.

SECTOR DETECTION

The sector detection circuit (figure 3-22) generates signals used to determine the angular position of the heads with respect to index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disks. The Sector pulses logically divide the disk into areas called sectors.

The Sector counter generates the Sector pulses; it generates a pulse each time it reaches its maximum count of 4095.

The counter is incremented by the 806 kHz clock pulses. These clock pulses are derived from the 9.67 MHz 1F Clock and represent the beginning of each data byte. The Index pulse resets the counter allowing 13 440 clock pulses per revolution of the disk.



NOTE
⚠1 THIS PULSE DOES NOT INCREMENT COUNTER BECAUSE INDEX IS STILL ACTIVE; THEREFORE, SECTOR 000 ALWAYS CONTAINS ONE MORE 806 kHz PULSE THAN ANY OTHER SECTOR.

9V73C

Figure 3-22. Sector Detection

The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution, up to a maximum count of 128. This is done by presetting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors, the counter would have to count 210 clock pulses in each sector (13 440 divided by 64) and the counter would be preset to 3886. In this case, the counter starts at 3886 and increments each clock time until it reaches the maximum count of 4095. Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (210) presets the counter back to 3886 (thus disabling the Sector pulse) and the counter begins the next sector.

The sector length is varied by presetting the sector select switches located on the card in logic chassis position B04/C04. Refer to section 1 of the maintenance manual (volume 1) for details regarding setting the sector switches.

HEAD SELECTION

Head selection must be preceded by a Cylinder Select (Seek) operation. The head selection logic shown in figure 3-23 can address any of the 40 (00 through 39) movable heads in the HDA, and also the fixed heads on units configured with the fixed head option. Once a specific head is selected, the current driver associated with the selected head allows the head to write on, or read from, the disk surface.

UNITS WITHOUT FIXED HEAD OPTION

A seek to cylinders 000 through 842 causes the servo logic to move the heads to the desired cylinder; it also enables movable head selection. Any attempt to seek to a cylinder beyond 842 generates a Seek Fault, disables head selection, and does not cause the servo logic to move the heads.

UNITS WITH FIXED HEAD OPTION

A seek to cylinders 000 through 842 causes the servo logic to move the heads to the desired cylinder; it also enables movable head selection. A seek to cylinders 896 through 898 enables fixed head selection: it is treated as a zero-track length seek by the servo logic. Any attempt to seek to cylinders 843 through 895 generates a Seek Fault, disables head selection, and does not cause the servo logic to move the heads.

READ/WRITE FUNCTIONS

GENERAL

Information is written on the disk surface using a modified frequency modulation (MFM) recording technique.

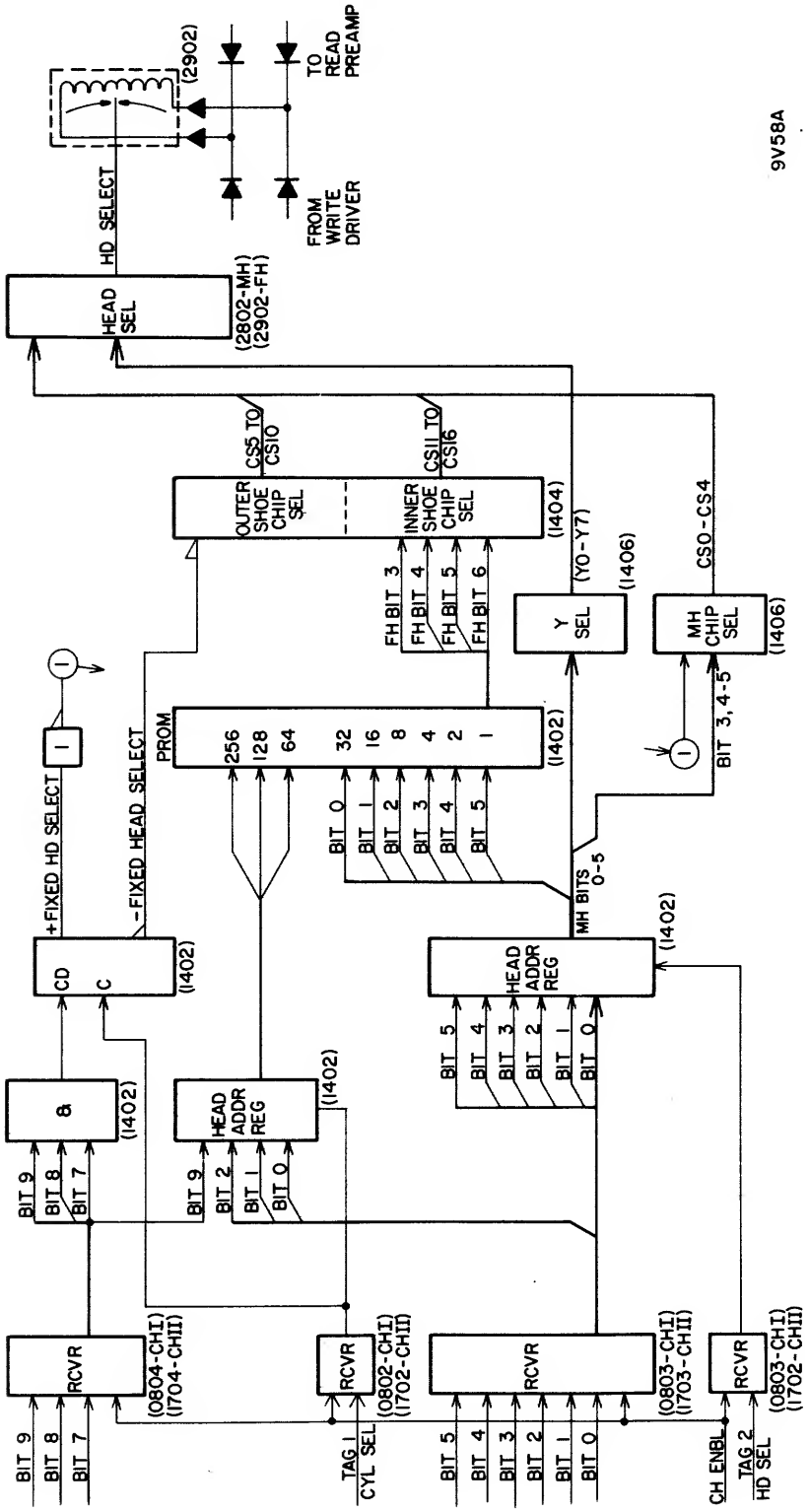


Figure 3-23. Head Selection

During Write operations, serial non-return-to zero (NRZ) digital data from the controller is converted into digital MFM data, and then into analog MFM data for writing on the disk surface.

During Read operations, the drive recovers analog MFM data from the disk surface, converts this information into digital MFM data, and then into digital NRZ data acceptable to the controller.

The drive is ready to perform either a Read or Write operation when it has completed a seek to the proper track and a head has been selected.

The controller initiates a Read or Write operation by sending a Control Select (Tag 3) along with the proper bus bit (Bit 0 for a Write operation or Bit 1 for a Read operation).

Both at the start and during a Read or Write operation, the drive checks for errors that would affect data as it is being read from, or written on, the disk.

Figure 3-24 shows the major components contained in the read/write circuits.

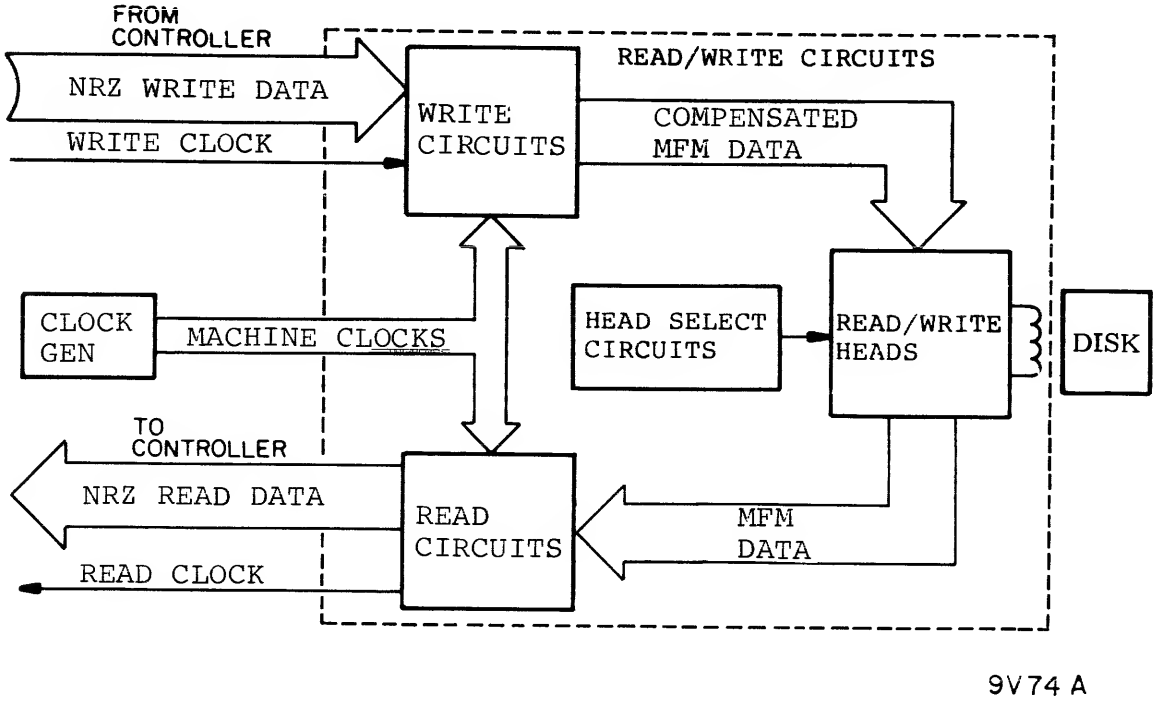


Figure 3-24. Read/Write Logic Block Diagram

NRZ/MFM RECORDING TECHNIQUES

Figure 3-25 provides a comparison of NRZ and MFM recording methods. The logic rules for each method are as follows:

NRZ Recording

- A binary "1" is recorded by a positive level during the cell time.
- A binary "0" is recorded by a negative level during the cell time.
- Transitions occur at the bit cell boundary between "01" and "10" combinations.

MFM Recording

- A binary "1" is recorded by a transition (positive or negative) at the center of the bit cell.
- A binary "0" is recorded by a constant level (positive or negative), at the center of the bit cell.
- There is a flux transition at the bit cell boundary between a "00" combination.
- There is no flux transition at the bit cell boundary between a "01" "10" or "11" combination.

READ CIRCUIT

General

Figure 3-26 illustrates the major components of the read circuit. Figure 3-27 illustrates typical device read timing parameters.

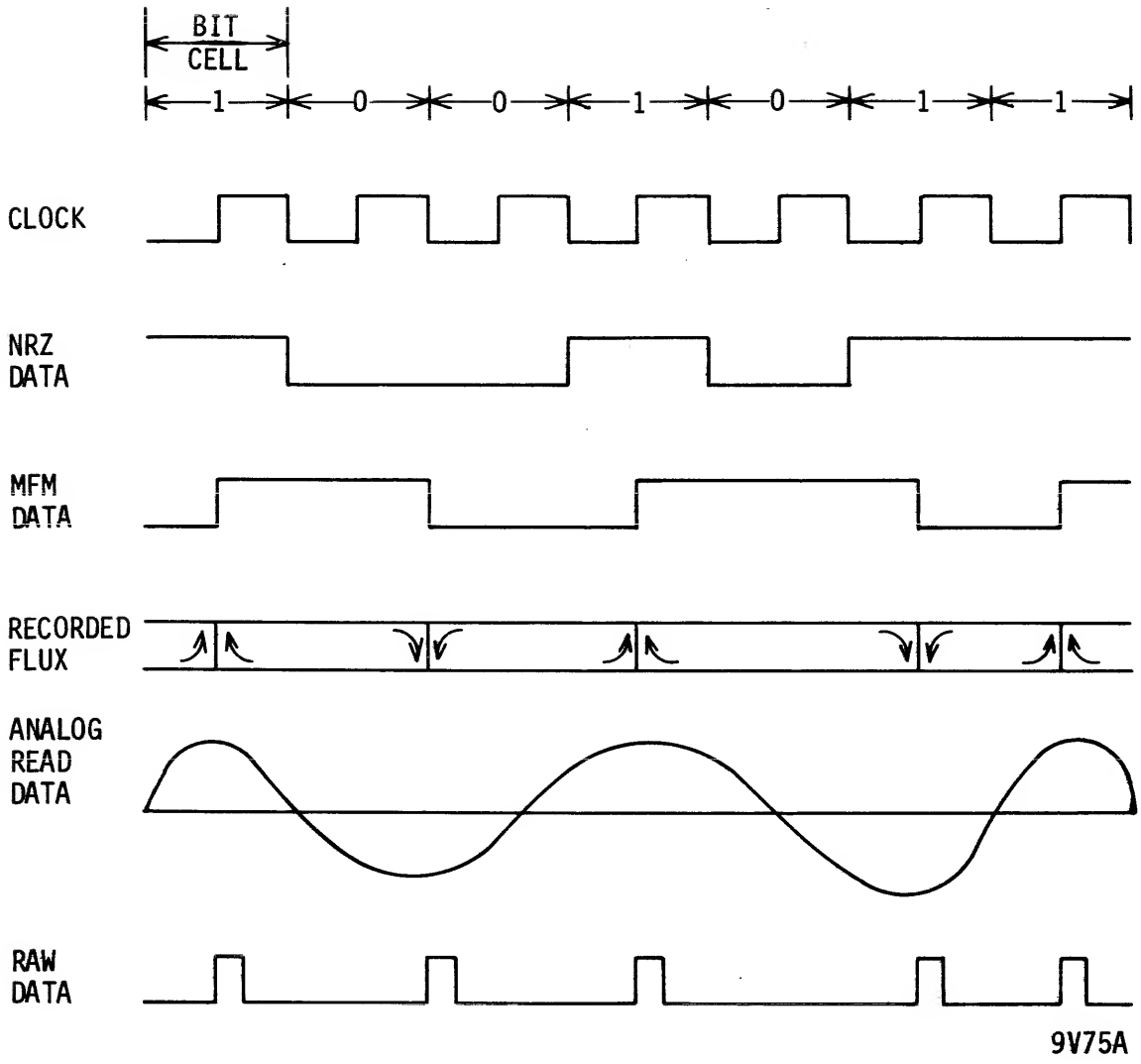


Figure 3-25. NRZ/MFM Recording

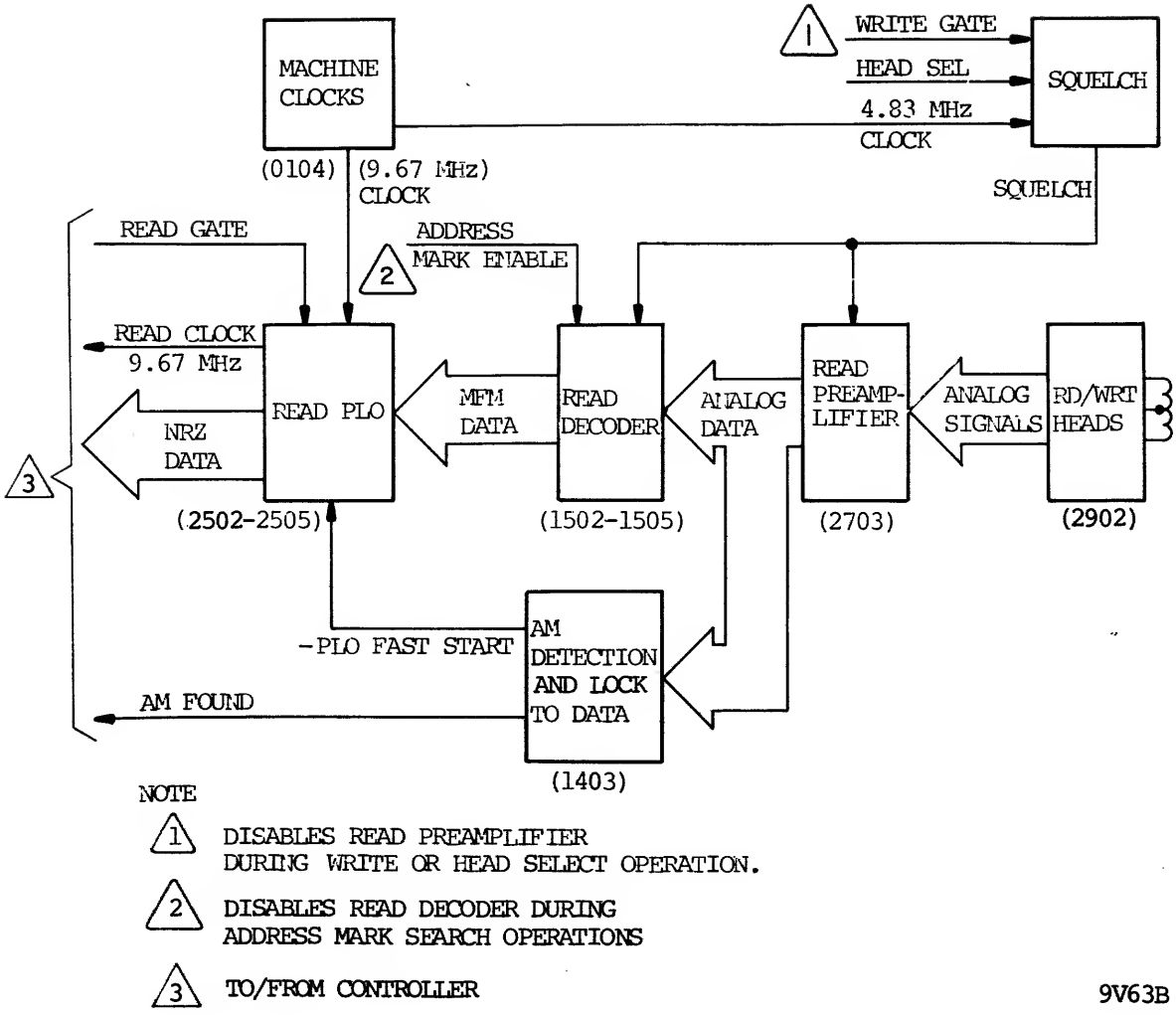


Figure 3-26. Read Logic

Read Preamplifier

The read preamplifier provides preliminary amplification of the analog voltage induced in the read/write head. This voltage is induced by the magnetic flux stored in the disk oxide during Write operations.

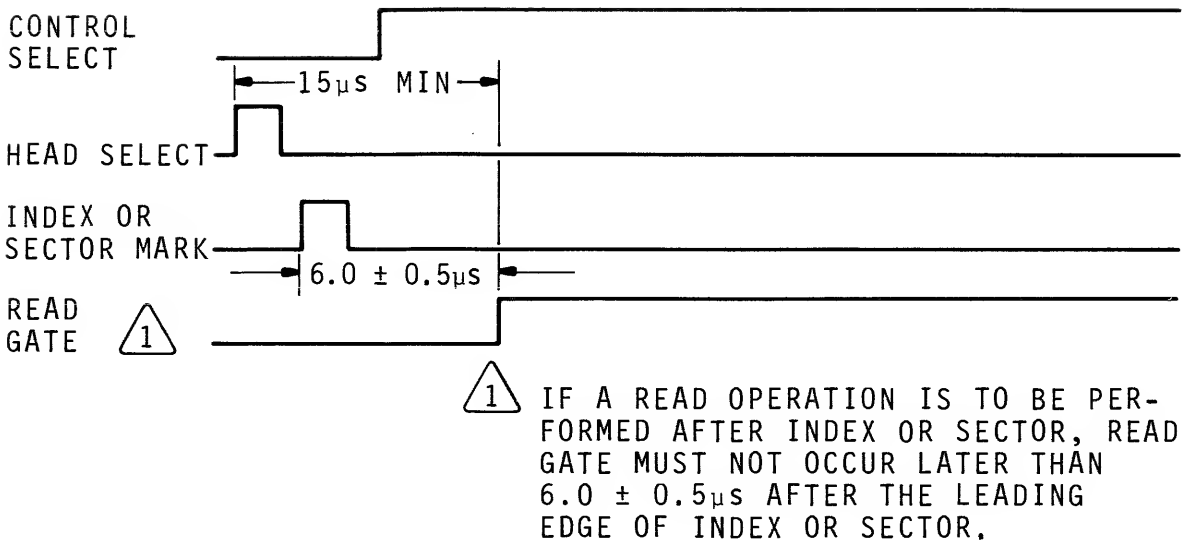


Figure 3-27. Read Timing

The preamplifier has three main parts: amplifier, squelch control and, low-gain control.

The input circuits of the amplifier are turned on at all times except when the drive is performing a write operation.

The Squelch signal prevents the amplifier from being overdriven by shorting the inputs (and therefore the transients) whenever the drive is performing a Write or Head Select operation.

In addition to the squelch control, the preamplifier also has a gain control circuit; it is used only when reading data received from a fixed head. This is called the low-gain control. Al-

though it reduces circuit gain, its effect is not as much as the squelch control. The low-gain control is necessary because the fixed heads are more sensitive than the movable heads. Without a gain reduction, Read signals from the fixed heads would overdrive the amplifier to distort the output.

The analog MFM output from the preamplifier is transmitted to the read decoder and to the AM Detect/Lock to Data circuitry.

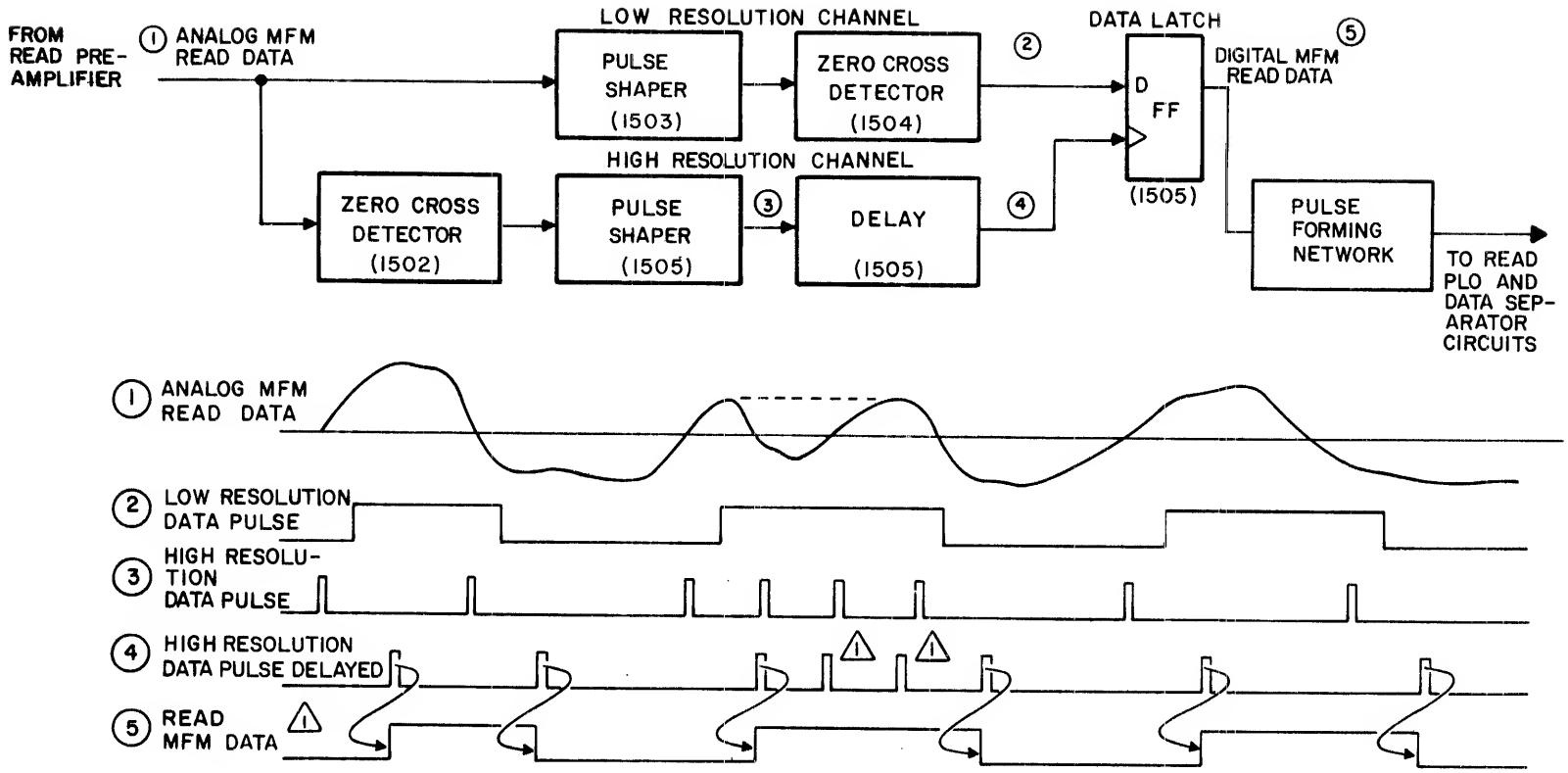
Read Decoder

The read decoder logic converts the analog MFM data from the read preamplifier to digital MFM data. This MFM data then goes to the read PLO, where it is converted to NRZ data and transmitted to the controller.

The analog-to-digital converter consists of high and low resolution data detection channels and a Data latch. The high and low-resolution channels monitor the analog MFM data and generate a digital pulse each time a data transition is detected. These pulses are then applied to the Data latch which uses them to produce digital MFM read data pulses.

The high-resolution channel generates signals that accurately define the leading and trailing edges of each MFM data transition. Because of its sensitivity, this channel can also produce false pulses caused by noise at its input. For this reason, a less sensitive low-resolution channel has been included. The low-resolution channel, although less accurate in detecting the transition points of the data, does not generate false outputs due to noise. Both high- and low-resolution signals are combined at the Data latch.

The output of the Data latch is processed by a pulse-forming network that produces 50-nanosecond pulses for each transition of the Data latch. The output of the network is digital MFM data as shown on figure 3-28.



NOTE:

⚠1 THESE DO NOT AFFECT DATA LATCH BECAUSE LOW RESOLUTION DATA PULSE DOES NOT CHANGE.

Figure 3-28. Read Decoder Logic

Two signals control operation of the analog-to-digital converter circuits: Squelch and Address Mark Enable Control.

The Squelch signal prevents the detection of transient pulses by disabling the logic during Write or Head Select operations. The Address Mark Enable signal prevents detection of transient pulses during Address Mark Search operations.

Lock to Data and AddressMark Detection

The PLO Fast Start signal synchronizes (Locks) the phase locked oscillator (PLO) to the read data from the disk surface. This signal is activated at the start of a read operation (Read Gate active) or whenever an address mark is detected while reading. It is disabled while searching for an address mark.

An address mark identifies the beginning of a data record on the track. It consists of a three-byte area that contains neither ones nor zeroes (2.4 @s with no data at all). The address mark detection logic is active only during read operations (tag 3 and Bus Out Bit 1 active). The controller activates the address mark detection circuitry by raising Bus Out Bit 5 (Address Mark Enable). The Address Mark Found signal is transmitted to the controller when an address mark is detected.

Read PLO

This circuitry has two functions. First, it converts the MFM data from the read decoder into NRZ data. Second, it generates a Read Clock that is synchronized to the frequency of the read data (9.67 MHz nominal). Both the NRZ data and the Read Clock signals are transmitted to the controller.

WRITE CIRCUIT

General

During a write operation, the controller sends NRZ data to the drive, which converts it to MFM, compensates the data for the effects of peak shift, calculates the proper amount of write current, and writes the data on the disk surface.

Figure 3-29 illustrates the major components of the write circuit; figure 3-30 illustrates typical write timing parameters.

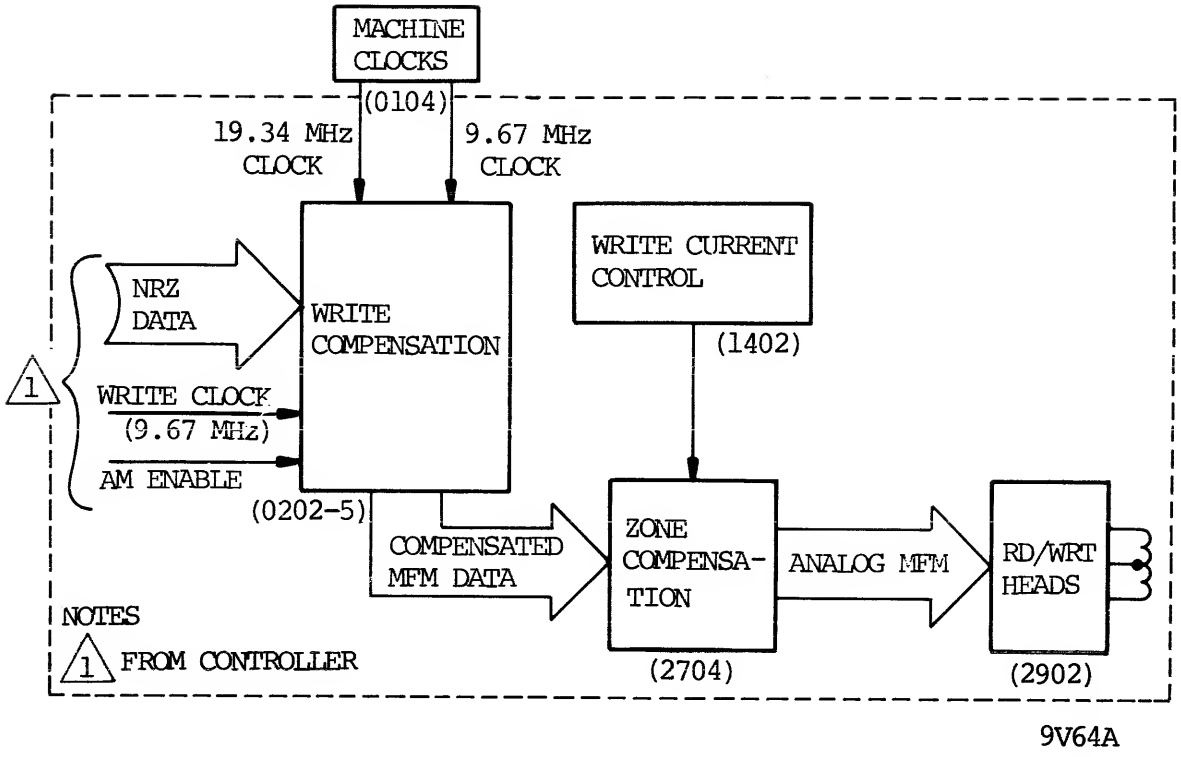


Figure 3-29. Write Logic

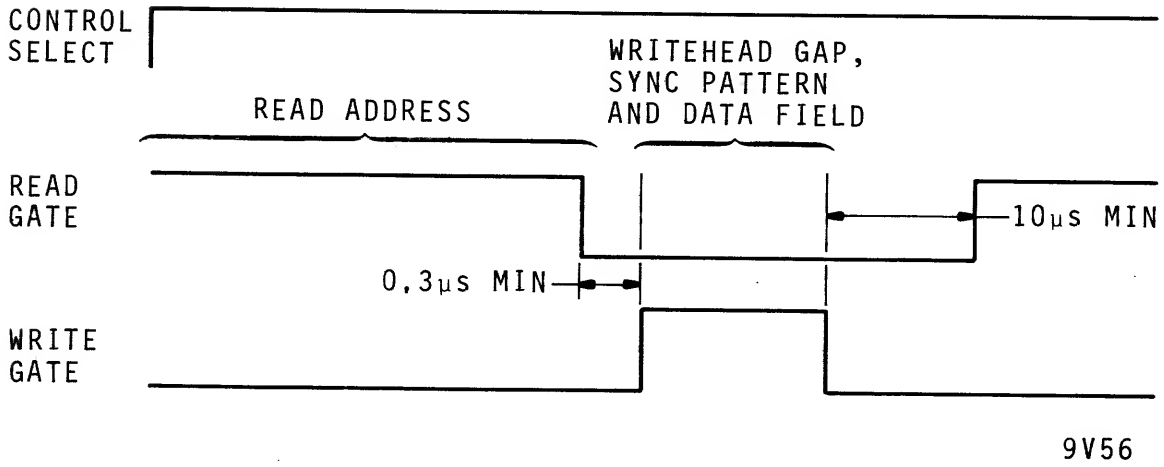


Figure 3-30. Write Timing

Write Compensation

The write compensation circuit converts NRZ data into MFM data while intentionally shifting the pulses in the data cell to compensate for peak shift.

Peak shift is a condition caused by variations in packing density of data on the disk. If the data being read is a "0" to "1" transition (decreasing frequency) the apparent readback peak will be later than normal. If the data being read is a "1" to "0" transition (increasing frequency), the apparent readback peak will be earlier than normal. No peak shift occurs if the frequency is constant (all "1"s or all "0"s pattern).

Zone Compensation

Write current zoning consists of using less current to write on the inner (higher number) tracks than the outer (lower number) tracks. Less current is used with the inner tracks because they have a smaller circumference and the data fits into a smaller area.

The write current zones are different depending upon whether the device is using fixed or movable heads.

Movable Head Zoning

The write current for movable heads divides into four zones (see figure 3-31): two for the odd heads and two for the even heads. In both cases the zones are from cylinder 000 to 512 and from cylinder 513 to 842.

Fixed Head Zoning

The write current for fixed heads divides into two zones (see figure 3-31). The first zone is for fixed heads 0 to 63 and the second for fixed heads 64-95.

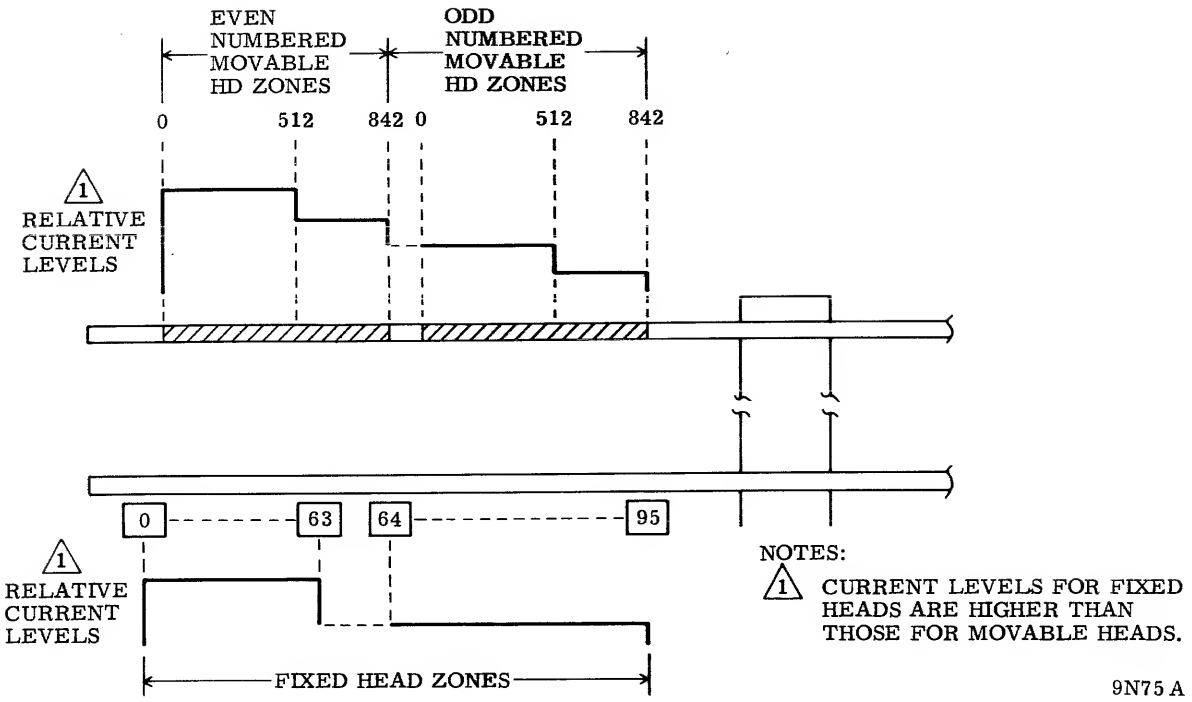


Figure 3-31. Write Current Zones

FIELD TEST UNIT (FTU) FUNCTIONS

The logic on the card in slot B02/C02 is used to check the dc voltage levels at the load and to duplicate the tests performed by the TB 216-A Field Test Unit.

Operating instructions for the FTU functions are contained in the Troubleshooting manual (Pub. No. 83323580).

PRELIMINARY REVISION PACKET. SUBJECT TO CHANGE WITHOUT NOTICE.

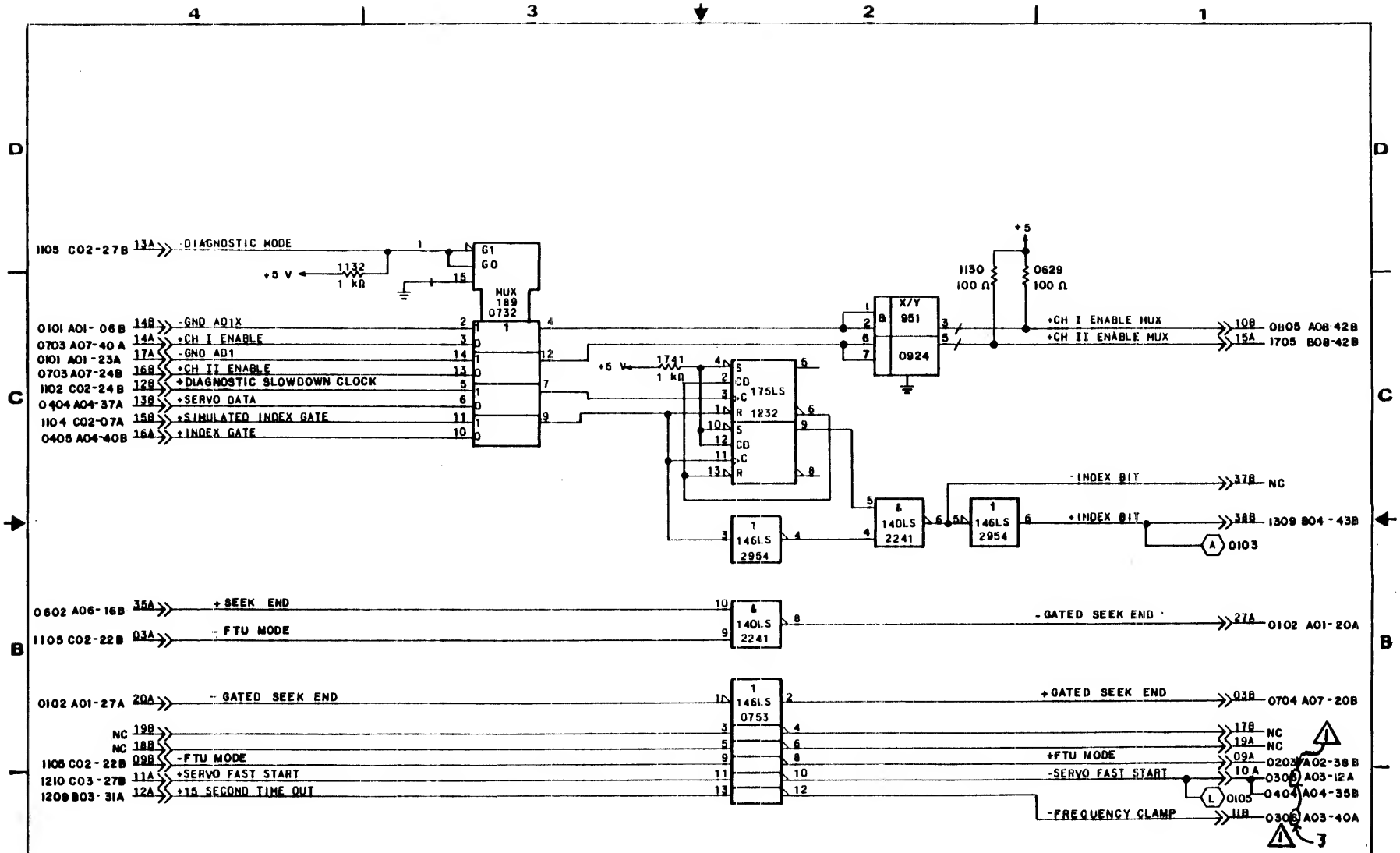
Publication Title: BZ7E1/BZ7E2 Hardware Maintenance Manual, Volume 2 of 2

Publication Number: 83323570 Manual Preliminary Revision: G

Instructions: The attached pages contain replacement information. Insert the attached pages into the appropriate place. Do not discard current manual sheet (back-up page information is not supplied with this packet). All changes contained in this preliminary packet will be in the released revision.

G1

REV	REWORK NUMBER	ECO/FCO NUMBER	DESCRIPTION	PAGES AFFECTED
01	C9068	DJ15090	Eliminate hybrid PLO chips. AKDX to BKDX.	1-24.2,1-24.4, 1-26,1-38.1 thru 1-38.7,1-42, 1-96.10,1-96.22

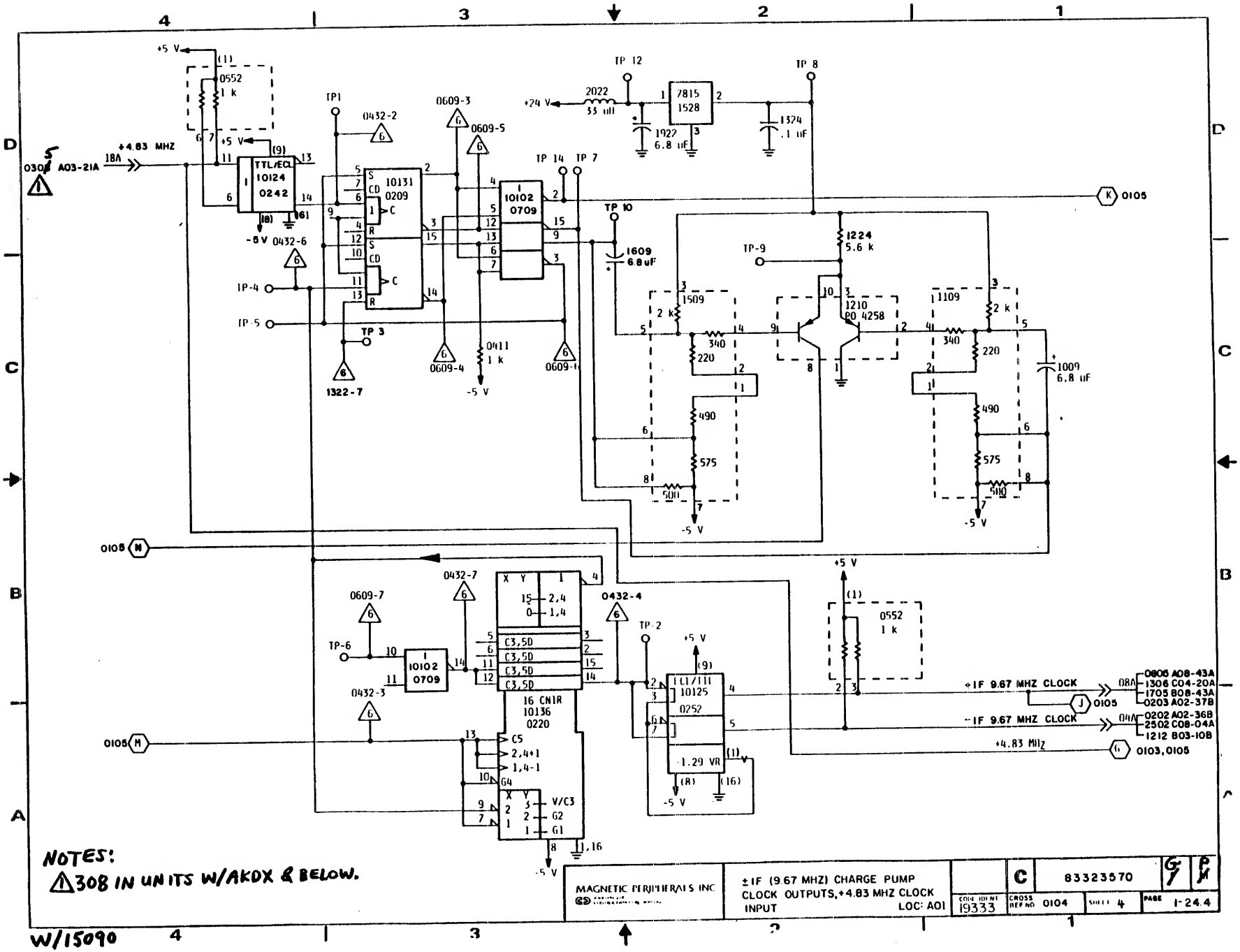


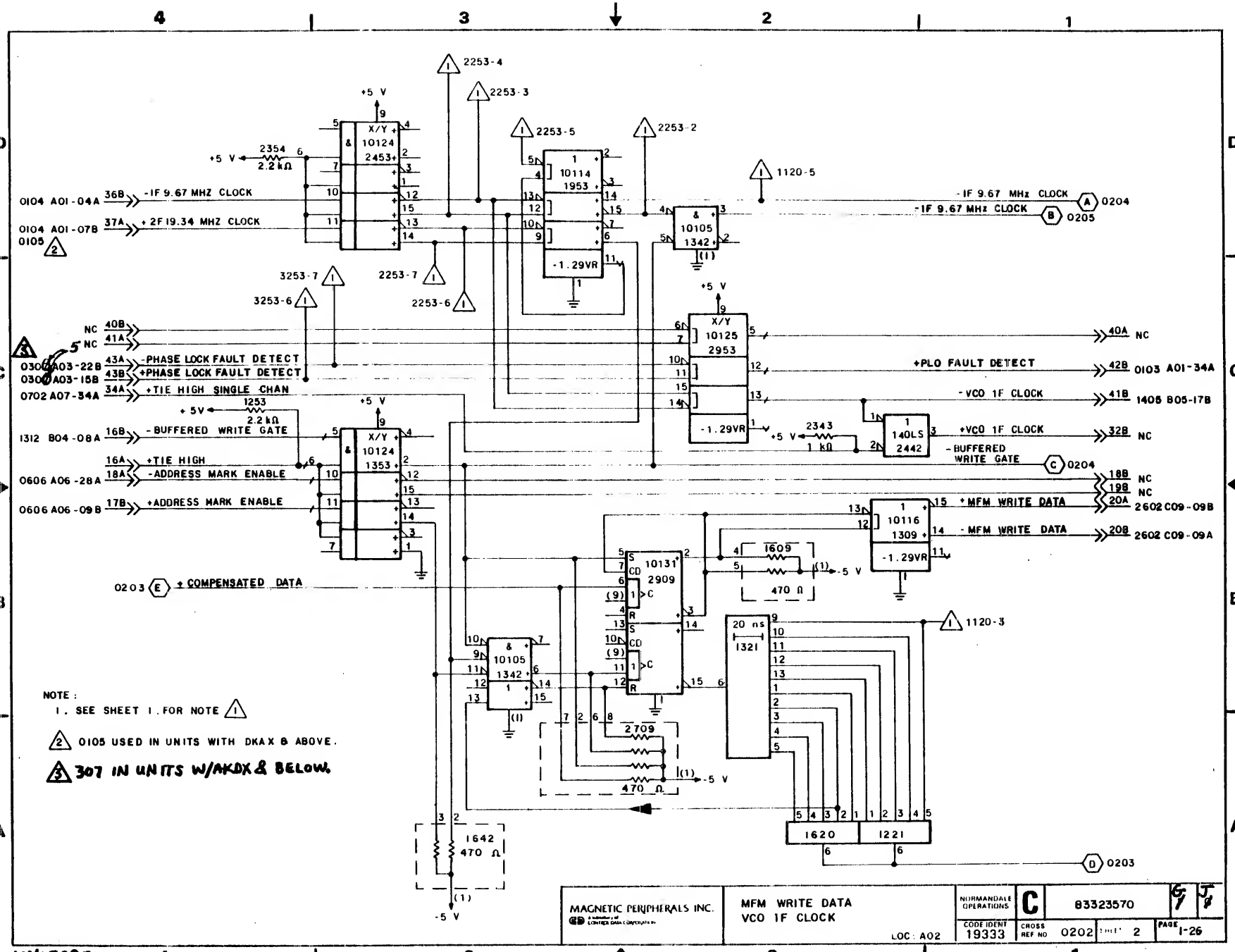
NOTES:

⚠1 306 IN UNITS W/AKDX & BELOW.

MAGNETIC PERIPHERALS INC.	CHAN MUX ENABLES, INDEX BIT GATE, FREQUENCY CLAMP LOC: A01		C	83323570	5	P/L
		CODE IDENT 19333	CROSS REF NO 0102	SHEET 2	PAGE 1-24.2	

W/15090


+5 V
0552
1 k
+4.83 MHZ
18A
0308 A03-21A
TTL/ECL
10124
0242
-5V 0432-6
TP1
0432-2
0609-3
0609-5
10131
0209
TP 12
TP 8
+24 V
2022
33 uH
7815
1528
1922
6.8 uF
1324
.1 uF
TP 14
TP 7
10102
0709
TP 10
1609
6.8uF
TP-9
1224
5.6 k
1509
2 k
340
220
490
575
500
1210
PD 4258
1109
1009
6.8 uF
TP-4
TP-5
TP 3
1322-7
0609-4
0411
1 k
-5 V
0105 K
0105 M
0432-7
0609-7
0432-4
TP-6
TP-2
0432-3
16 CNTR
10136
0220
C3,5D
C5
2,4+1
1,4-1
V/C3
G2
G1
C1/11
10125
0252
1.29 VR
+1F 9.67 MHZ CLOCK
-1F 9.67 MHZ CLOCK
+4.83 MHz
0105 J
0103,0105 G
0806 A08-43A
1306 C04-20A
1705 B08-43A
0203 A02-37B
0202 A02-36B
2502 C08-04A
1212 B03-10B
NOTES:
⚠308 IN UNITS W/AKDX & BELOW.
MAGNETIC PERIPHERALS INC
±1F (9.67 MHZ) CHARGE PUMP CLOCK OUTPUTS,+4.83 MHZ CLOCK INPUT
LOC: A01
C
83323570
CODE IDENT 19333
CROSS REF NO 0104
SHEET 4
PAGE 1-24.4
W/15090


0104 A01-04A 36B -IF 9.67 MHZ CLOCK
0104 A01-07B 37A +2F 19.34 MHZ CLOCK
0105 (2)
+5 V
2354 2.2 kΩ
X/Y 10124 2453
2253-4
2253-3
2253-5
2253-2
1120-5
1 10114 1953
-1.29VR
& 10105 1342 (1)
-IF 9.67 MHz CLOCK (A) 0204
-IF 9.67 MHz CLOCK (B) 0205
3253-7
3253-6
2253-7
2253-6
(3) 5
NC 40B
NC 41A
0300 A03-22B -PHASE LOCK FAULT DETECT 43A
0300 A03-15B +PHASE LOCK FAULT DETECT 43B
0702 A07-34A +TIE HIGH SINGLE CHAN 34A
X/Y 10125 2953
-1.29VR
40A NC
+PLO FAULT DETECT 42B 0103 A01-34A
-VCO 1F CLOCK 41B 1405 B05-17B
2343 1 kΩ
1 140LS 2442
+VCO 1F CLOCK 32B NC
-BUFFERED WRITE GATE (C) 0204
1253 2.2 kΩ
1312 B04-08A 16B -BUFFERED WRITE GATE
X/Y 10124 1353
16A +TIE HIGH
0606 A06-28A 18A -ADDRESS MARK ENABLE
0606 A06-09B 17B +ADDRESS MARK ENABLE
18B NC
19B NC
1 10116 1309 -1.29VR
+MFM WRITE DATA 20A 2602 C09-09B
-MFM WRITE DATA 20B 2602 C09-09A
1609 470 Ω (1) -5 V
0203 (E) +COMPENSATED DATA
10131 2909
& 10105 1342 (1)
20 ns 1321
1120-3
2709 470 Ω (1) -5 V
1642 470 Ω (1) -5 V
1620
1221
(D) 0203
NOTE :
1. SEE SHEET 1. FOR NOTE (1)
(2) 0105 USED IN UNITS WITH DKAX & ABOVE.
(3) 307 IN UNITS W/AKDX & BELOW.
MAGNETIC PERIPHERALS INC.
MFM WRITE DATA
VCO 1F CLOCK
LOC: A02
NORMANDALE OPERATIONS
C
83323570
CODE IDENT 19333
CROSS REF NO 0202
SHEET 2
PAGE 1-26
W/15090

REVISION STATUS OF SHEETS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	A	A	A	A	A	A	A												
B		B	B																
C						C													
D	D																		
E					E		E												
F	F	F	F	F	F	F													

SPARE TERMINATORS

0528	- 2, 6
0599	- 4, 6
0917	- 2, 5, 7
0939	- 6, 7
1339	- 2
1869	- 3, 4
3050	- 2, 7

DELETE

FILTER CAPS (2)

.1 uF	
+5 V	-5 V
-0261	-0226
-0748	-0516
-2716	-0626
-2948	-0837
	-1148
	-1237
	-1516
	-1526
	-1837
	-1948
	-2116
	-2448
	-2526
	-2926

UNUSED DEVICES

Q PACK-1940-8,9,10
R PACK-1928-5,6
1939-1,2,5,6
2528-5,6,7,8

SPARE GATES

LOC.	TYPE	INPUT	OUTPUT
3139	10102	4, 5	2
1017	10102	6, 7	3
		12, 13	9, 15

REVISIONS

REV	ECO	DESCRIPTION	DRFT	DATE	CHK'D
A	PE81000	RELEASED	CB	1-10-80	
B	PE81138	ADD CARD CNB	TH	7-14-80	
C	PE81163	ADD FTU CAPABILITIES	TH	9-3-81	
D	PE81736	UPDATE LOGIC DIAG'S	CB	10-15-80	
E	PE81804	UPDATE LOGIC DIAG'S	CB	4-7-81	

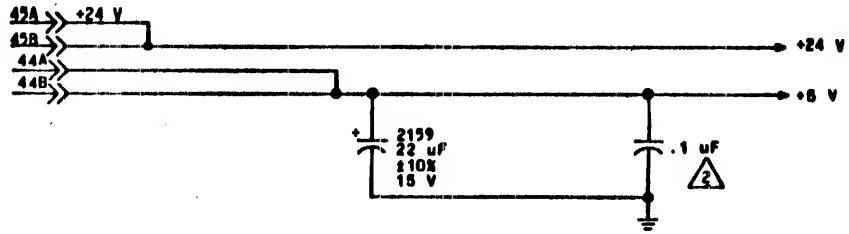
NOTES:

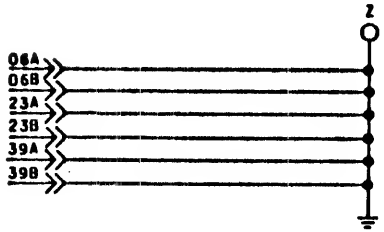
(1) UNLESS OTHERWISE SPECIFIED:

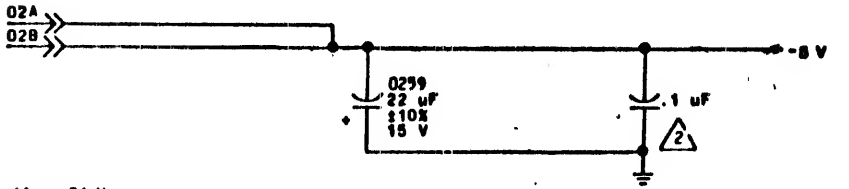
ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5 V.

(2) SEE TABLE FOR .1μF CAPACITOR LOCATIONS

(3) TYPICAL TERMINATOR CONFIGURATION.

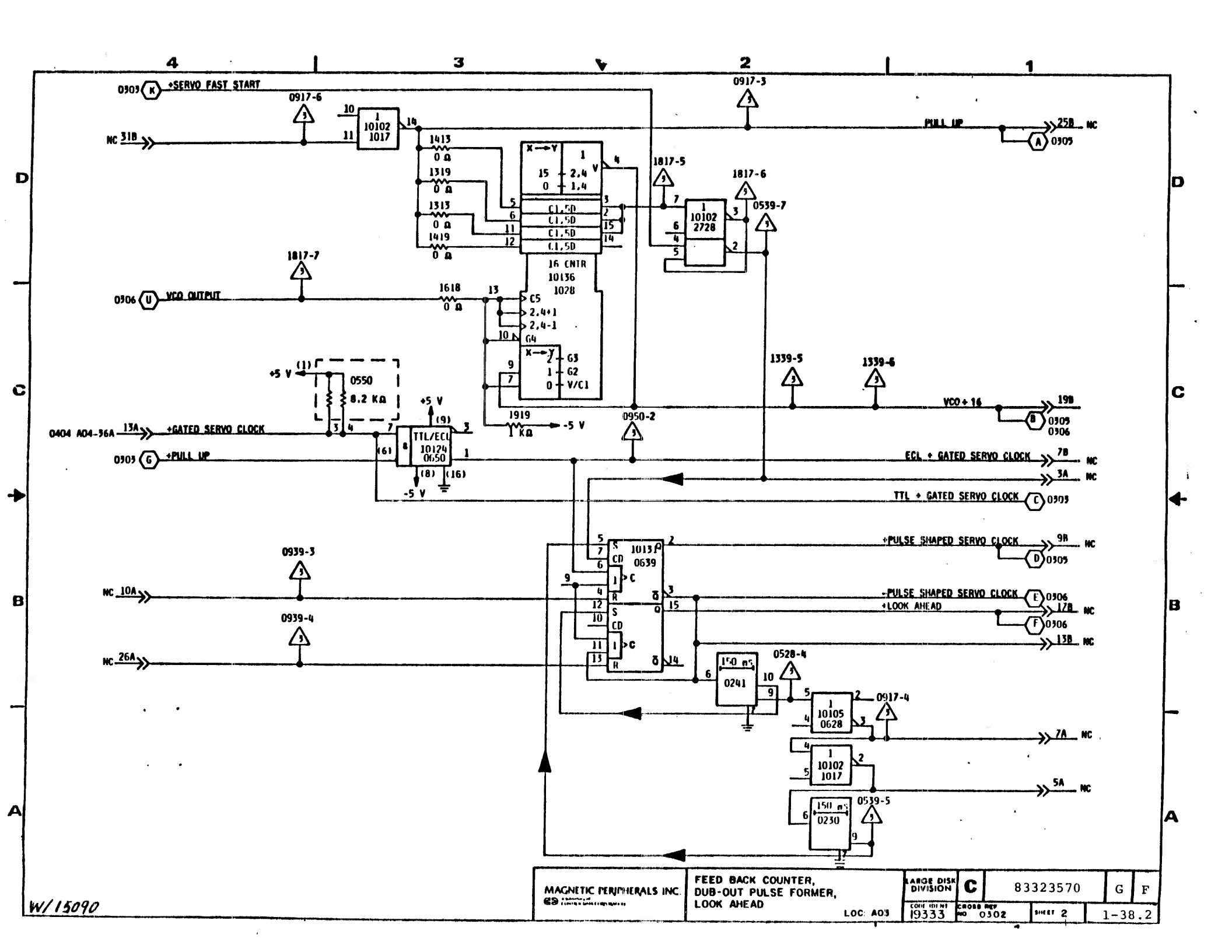


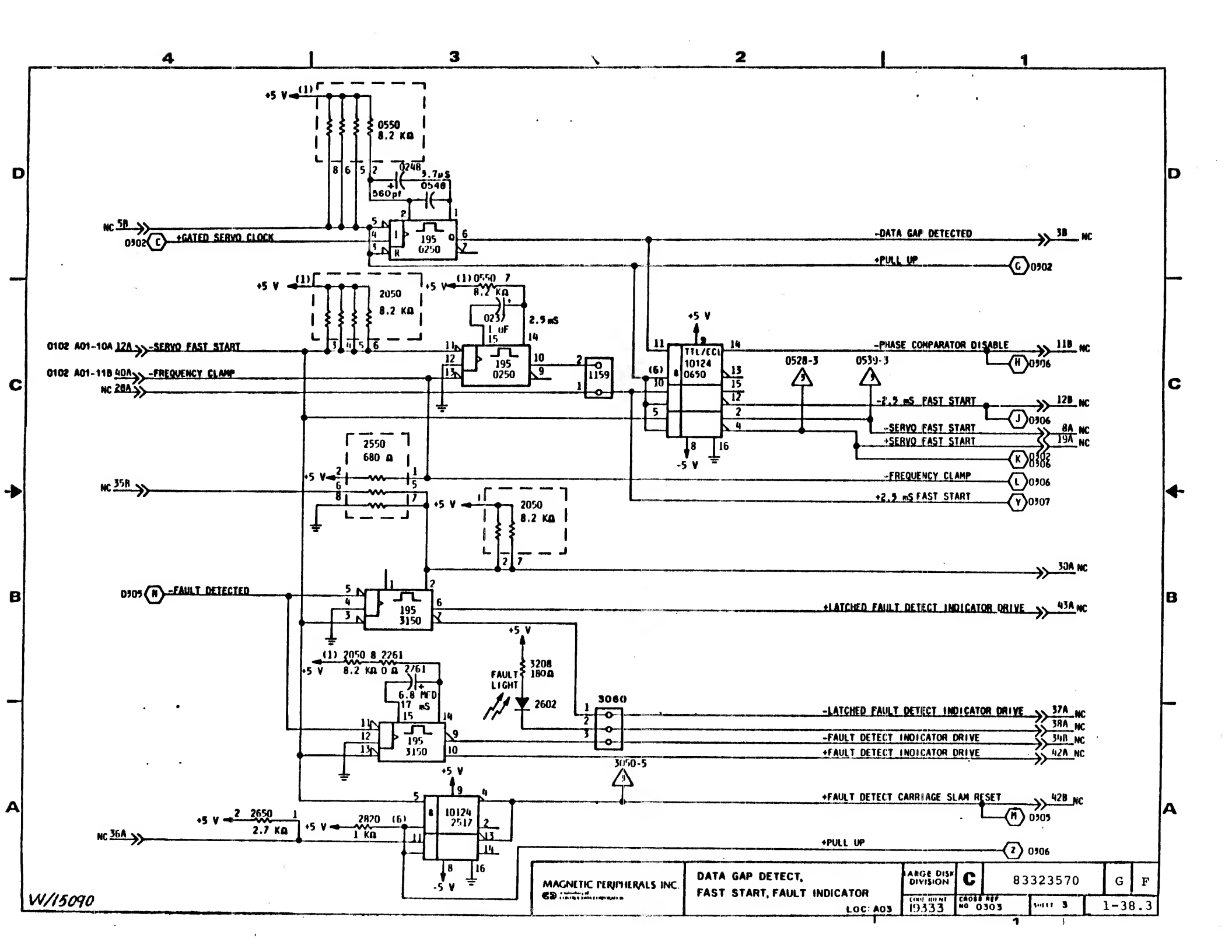


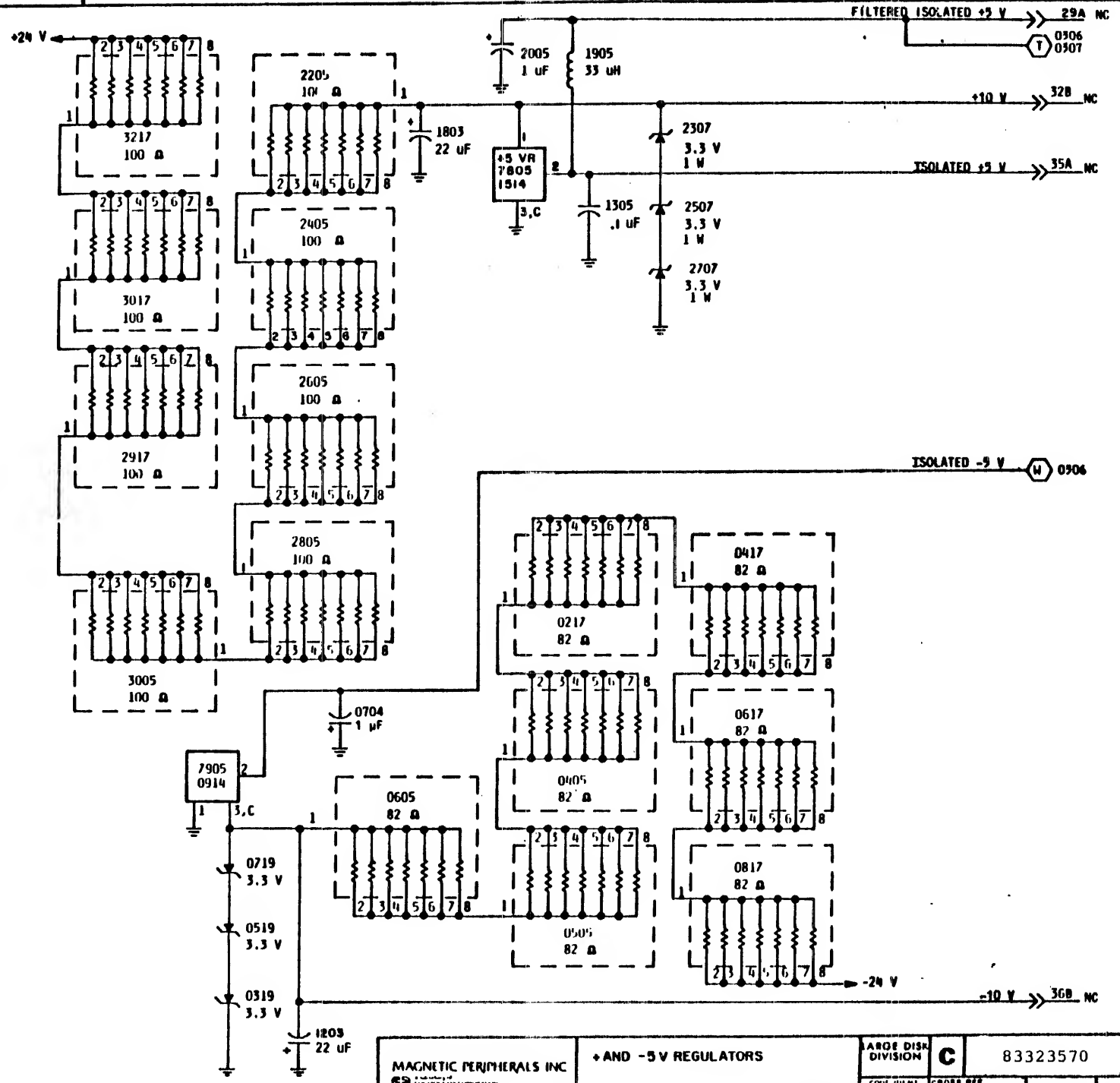


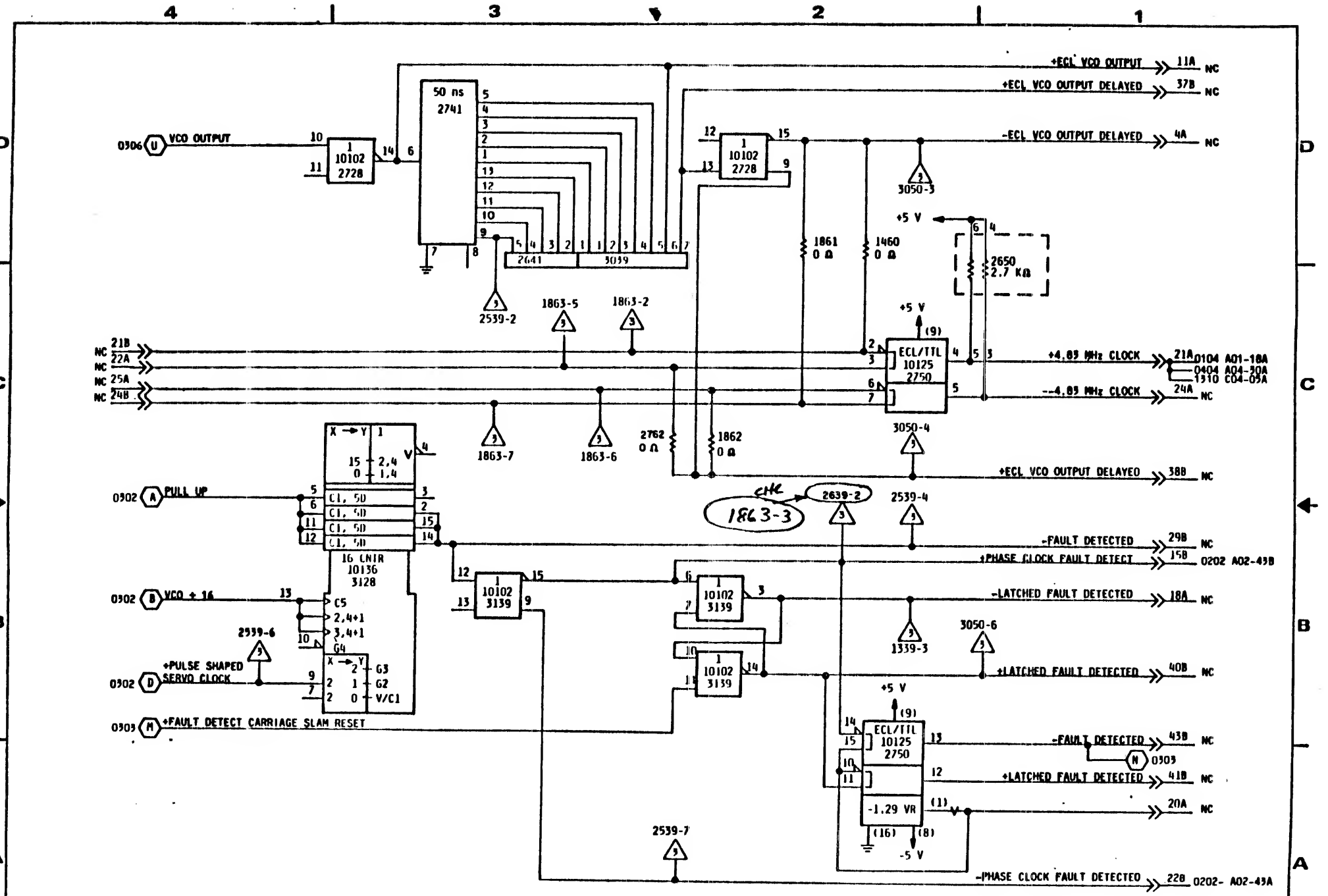
DRAWN	M. Anderson	3/19/80	MAGNETIC PERIPHERALS INC.	SERVO PLO DIAGRAMS	NORMANDALE OPERATIONS	C	83323570	G	F
CHECKED									
ENGINEER	D.S. Reed	4/14/80		TYPE: BKDX LOC: A03	CODE IDENT 19333	USED REF NO 0301	SHEET 1 OF 7	PAGE 1-38.1
APPROVED									

W/15090


4
3
2
1
D
C
B
A
0909 K +SERVO FAST START
0917-6
0917-3
NC 31B
1 10102 1017
1413 0 Ω
1319 0 Ω
1313 0 Ω
1419 0 Ω
X→Y 1 V
15 2,4
0 1,4
C1,5D
C1,5D
C1,5D
C1,5D
1817-5
1817-6
1 10102 2728
0539-7
PULL UP
25B NC
A 0909
1817-7
0906 U VCO OUTPUT
1618 0 Ω
16 CNTR 10136 1028
C5
2,4+1
2,4-1
G4
X→Y
G3
G2
V/C1
1339-5
1339-6
VCO÷16
19B
B 0909 0906
+5 V
0550 8.2 KΩ
1919 1 KΩ
-5 V
0950-2
0404 A04-36A 13A +GATED SERVO CLOCK
0909 G +PULL UP
TTL/ECL 10124 0650
ECL ÷ GATED SERVO CLOCK
7B NC
3A NC
TTL ÷ GATED SERVO CLOCK
C 0909
0939-3
NC 10A
0939-4
NC 26A
1013 0639
+PULSE SHAPED SERVO CLOCK
9B NC
D 0909
-PULSE SHAPED SERVO CLOCK
E 0906
+LOOK AHEAD
17B NC
F 0906
13B NC
150 ns 0241
0528-4
0917-4
1 10105 0628
7A NC
1 10102 1017
5A NC
150 ns 0230
0539-5
W/15090
MAGNETIC PERIPHERALS INC.
FEED BACK COUNTER, DUB-OUT PULSE FORMER, LOOK AHEAD
LOC: A03
LARGE DISK DIVISION
C
83323570
G
F
CODE IDENT 19333
CROSS REF NO 0302
SHEET 2
1-38.2

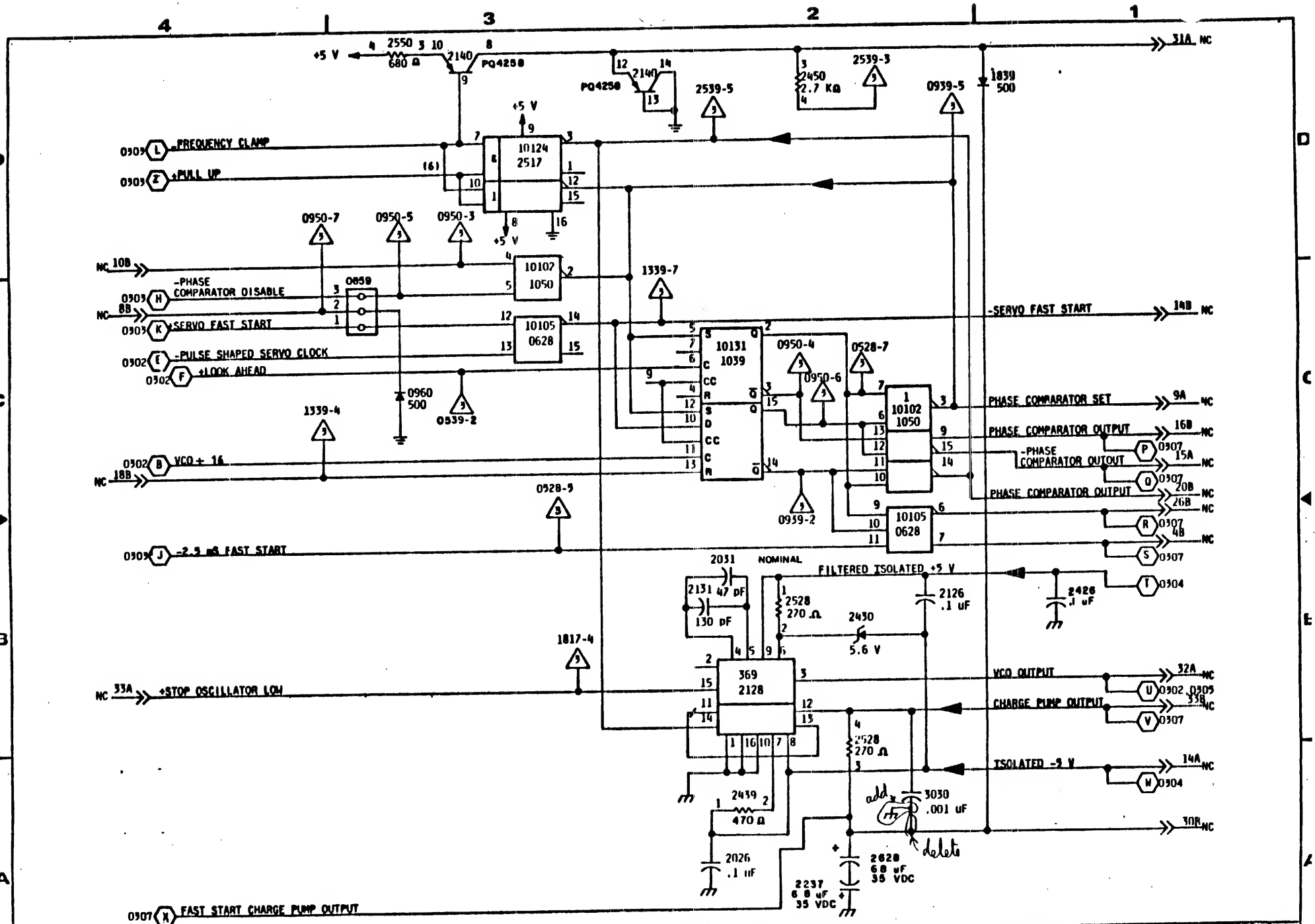

4
3
2
1
D
C
B
A
+5 V
0550
8.2 KΩ
0248
560pf
3.7mS
0548
NC 5B
0902 C +GATED SERVO CLOCK
195
0250
-DATA GAP DETECTED 3B NC
+PULL UP G 0902
2050
8.2 KΩ
0550 7
8.2 KΩ
0237
1 uF
2.9 mS
0102 A01-10A 12A -SERVO FAST START
0102 A01-11B 40A -FREQUENCY CLAMP
NC 28A
1159
TTL/ECL
10124
0650
0528-3
0539-3
-PHASE COMPARATOR DISABLE 11B NC
H 0906
-2.9 mS FAST START 12B NC
J 0906
-SERVO FAST START 8A NC
+SERVO FAST START 19A NC
K 0902 0906
-FREQUENCY CLAMP L 0906
+2.5 mS FAST START Y 0907
-5 V
2550
680 Ω
NC 35B
30A NC
0905 N -FAULT DETECTED
195
3150
+LATCHED FAULT DETECT INDICATOR DRIVE 43A NC
(1) 2050 & 2261
8.2 KΩ 0 Ω 2761
6.8 MFD
17 mS
FAULT LIGHT
3208
180Ω
2602
3060
-LATCHED FAULT DETECT INDICATOR DRIVE 37A NC
38A NC
-FAULT DETECT INDICATOR DRIVE 34B NC
+FAULT DETECT INDICATOR DRIVE 42A NC
3050-5
+FAULT DETECT CARRIAGE SLAM RESET 42B NC
M 0905
2650
2.7 KΩ
2820
1 KΩ
10124
2517
NC 36A
+PULL UP Z 0906
W/15090
MAGNETIC PERIPHERALS INC.
DATA GAP DETECT,
FAST START, FAULT INDICATOR
LOC: A03
LARGE DISK DIVISION
C
83323570
G F
CONTRACT NO 19333
CROSS REF NO 0303
SHEET 3
1-38.3


4
3
2
1
D
C
B
A
+24 V
3217
100 Ω
3017
100 Ω
2917
100 Ω
3005
100 Ω
2205
100 Ω
2405
100 Ω
2605
100 Ω
2805
100 Ω
1803
22 uF
2005
1 uF
1905
33 uH
+5 VR
7805
1514
3,C
1305
.1 uF
2307
3.3 V
1 W
2507
3.3 V
1 W
2707
3.3 V
1 W
FILTERED ISOLATED +5 V
29A NC
0306
0307
+10 V
32B NC
ISOLATED +5 V
35A NC
ISOLATED -5 V
0306
0704
1 μF
7905
0914
0605
82 Ω
0217
82 Ω
0405
82 Ω
0505
82 Ω
0417
82 Ω
0617
82 Ω
0817
82 Ω
-24 V
-10 V
36B NC
0719
3.3 V
0519
3.3 V
0319
3.3 V
1203
22 uF
MAGNETIC PERIPHERALS INC
+AND -5 V REGULATORS
LOC: A03
LARGE DISK DIVISION
C
83323570
G
F
CODE IDENT 19333
CROSS REF NO 0304
SHEET 4
1-38.4
W/15090



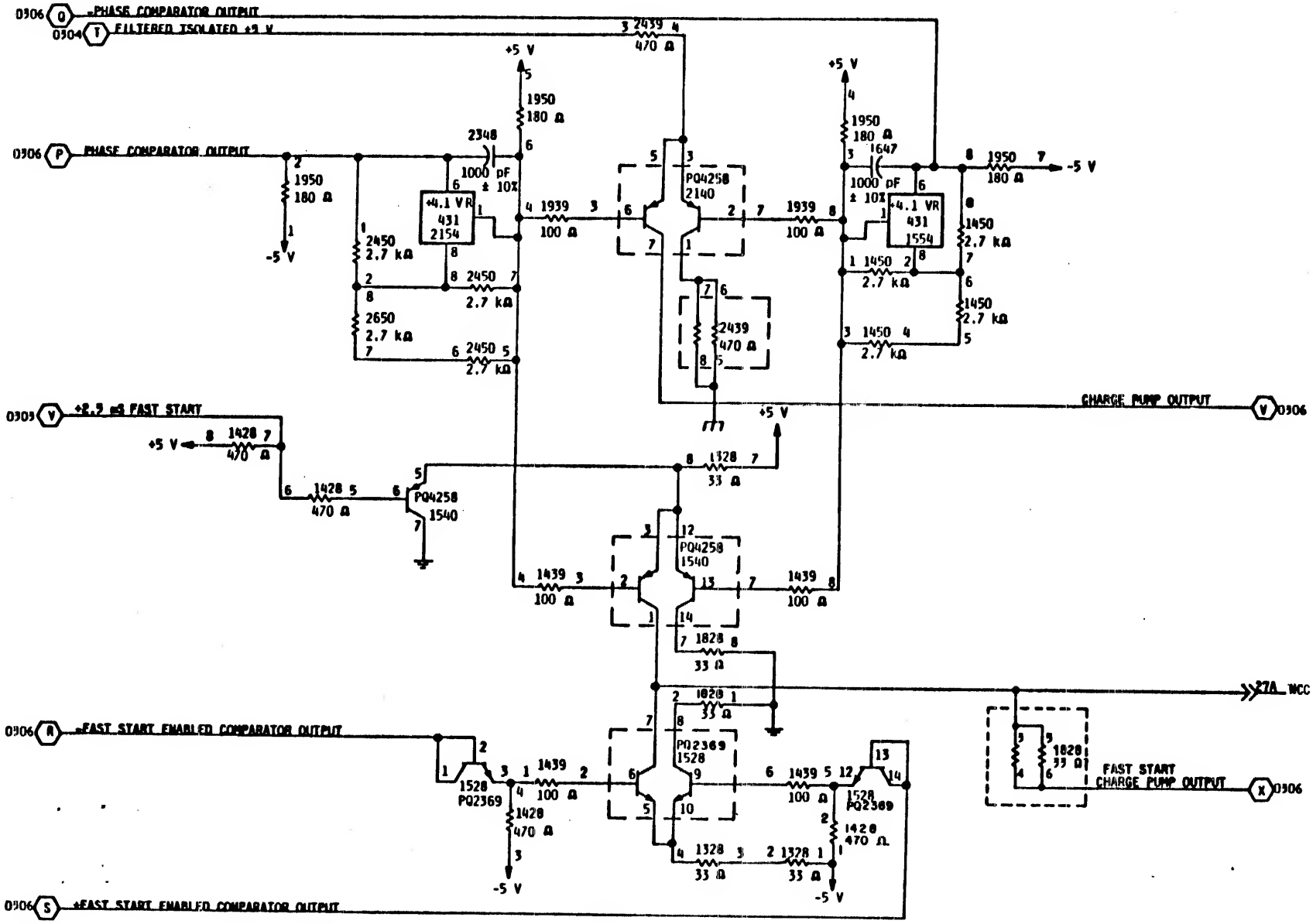
MAGNETIC PERIPHERALS INC.	OUTPUT CIRCUITRY FAULT DETECT	LARGE DISK DIVISION	C	83323570	G	F
	LOC: A03	CODE IDENT 19333	CROSS REF NO 0305	SHEET 5	1-38.5	

W/15090



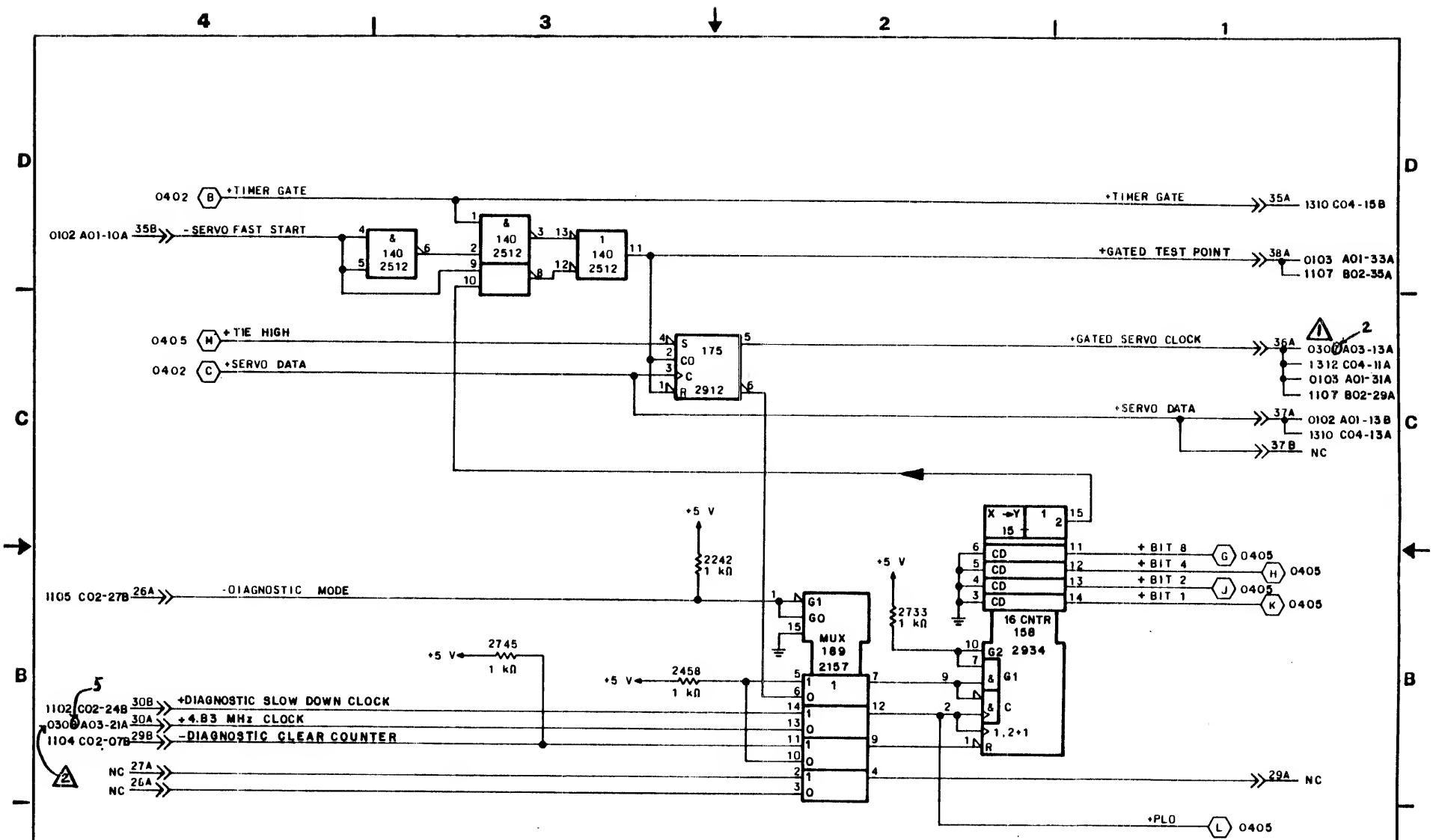
MAGNETIC PERIPHERALS INC	PHASE COMPARATOR, VCO	LARGE DISK DIVISION	C	83323570	G F
	LOC: A03	CODE IDENT 19333	CROSS REF NO 0306	SHEET 6	1-38.6

W/15090



MAGNETIC PERIPHERALS INC.	CHARGE PUMP, FAST START CHARGE PUMP LOC: A03	LARGE DISK DIVISION	C	83323570	G	F
		CDC IDENT 19333	CROSS REF NO 0307	SHEET 7	1-38.7	

W/15090

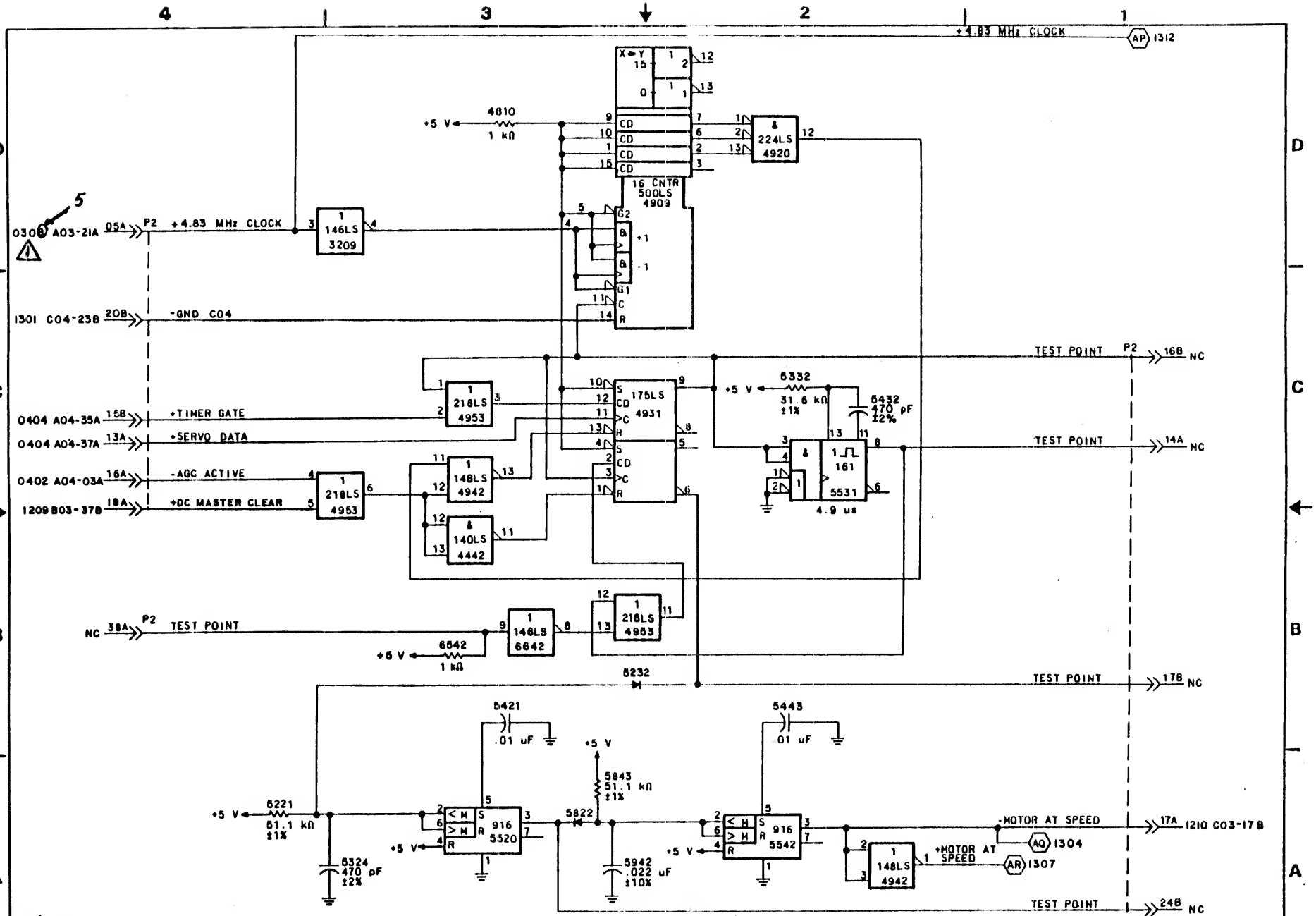


NOTES:

1. 307 IN UNITS W/AKDX & BELOW
2. 308 IN UNITS W/AKDX & BELOW.

MAGNETIC PERIPHERALS INC.	TIMER GATE, GATED SERVO CLOCK, SERVO DATA, PLO CLOCK COUNTER LOC: A04	NORMANDALE OPERATIONS	C	83323570	
		CODE IDENT 19333	CROSS REF NO 0404	SHEET 4	PAGE 1-42

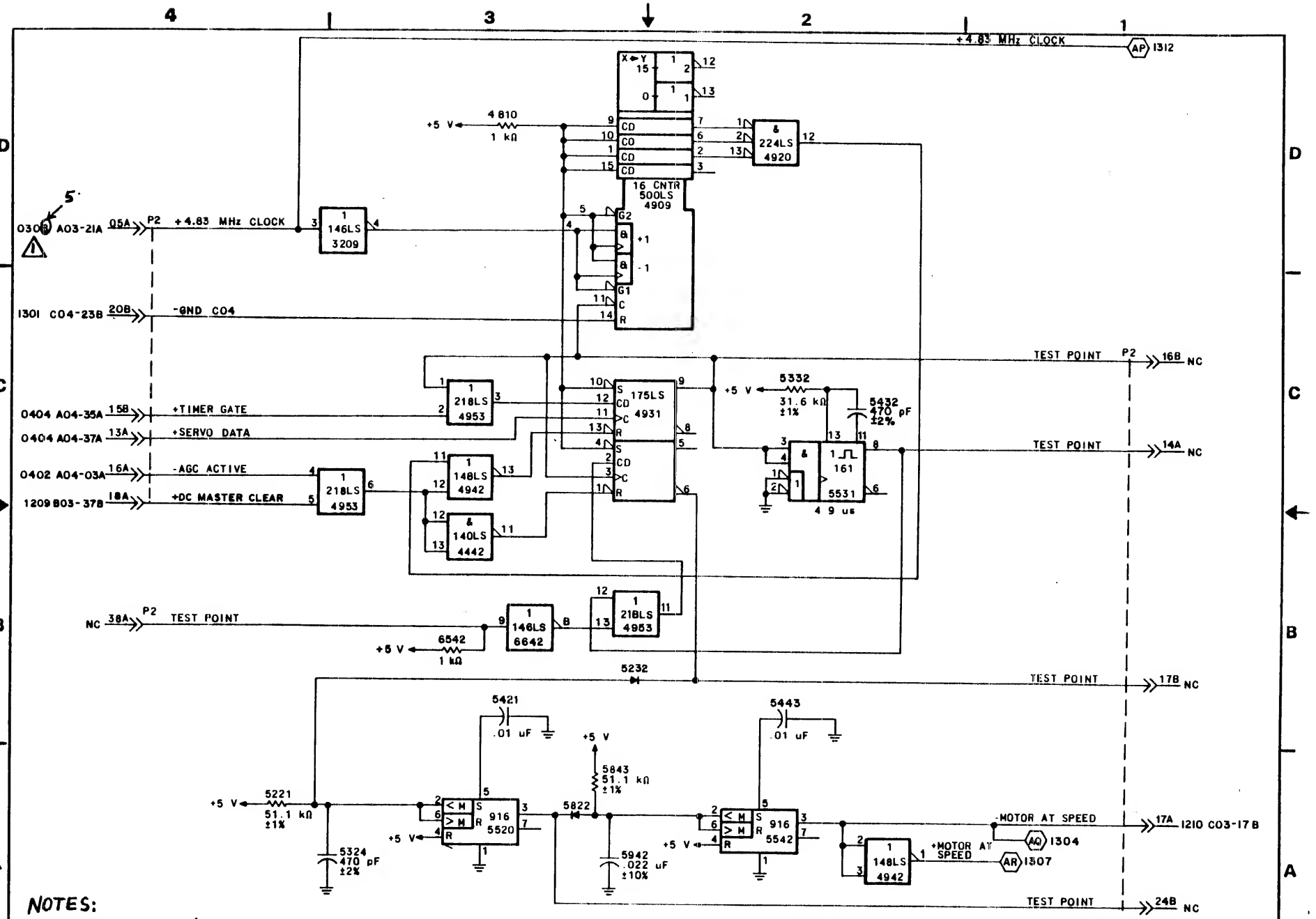
w/15090



NOTES:
⚠308 IN UNITS W/AKDX & BELOW.

MAGNETIC PERIPHERALS INC.	MOTOR AT SPEED DETECTION	LARGE DISK DIVISION C	83323570
	LOC: B04/C04	CODE IDENT 19333	CROSS REF NO 310 · SHEET 10 · PAGE 1-96.10

W/15090



NOTES:

⚠ 308 IN UNITS W/AKDX & BELOW.

MAGNETIC PERIPHERALS INC.	MOTOR AT SPEED DETECTION	NORMANDALE OPERATIONS	C	83323570	G R
	LOC: B04/C04	CODE IDENT 19333	CROSS REF No! 310	SHEET 10	PAGE 1-96.22

W/15090

COMMENT SHEET

MANUAL TITLE:

PUBLICATION NO.: **REVISION:**

NAME: _____

COMPANY: _____

STREET ADDRESS: _____

CITY: _____ **STATE:** _____ **ZIP CODE:** _____

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